

Basic Four[®] Model 4403 (Machine Type TBD) ¹/4 Inch Magnetic Cartridge Streamer Service Manual





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This is only to support people who collect historic computers.

This comment is the only change to the Servive Manual, other contents are unchanged.

Armin 2005/10/01



Basic Four Information Systems

Basic Four® Model 4403 (Machine Type TBD) ¹/4 Inch Magnetic Cartridge Streamer Service Manual

August 1984

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PREFACE

This manual provides service information for the Model 4403 Magnetic Cartridge Streamer (Machine Type TBD). The information is presented as an aid for field service personnel, and supports the installation, operation, and maintenance of the device.

The major topics covered in this manual are:

Section	I	Introduction
Section	II	Installation
Section	III	Functional Description
Section	IV	Maintenance
Section	V	Removal/Replacement
Section	VI	Illustrated Parts List
Section	VII	Reference Data
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WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications, as temporarily permitted by regulation. It has not been tested for compliance with the limits for Class A Computing Devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the User at his own expense will be required to take whatever measures that may be required to correct the interference. BFSID 8082



SECTION I

INTRODUCTION

1.1 GENERAL DESCRIPTION

The Model 4403 Magnetic Cartridge Streamer (MCS), shown in figure 1-1, is a microprocessor controlled, 1/4-inch cartridge tape drive system. The MCS only operates in the streaming (continuous) mode, specifically designed as a fixed disk memory backup. The MCS conforms to the QIC-02 Intelligent Interface Standard and QIC-24 Data Interchange Format Standard for compatibility with most host systems.

The MCS read/write speed is 90 inches per second (ips). Nine tracks of data are recorded in a serpentine format. All recorded tracks are verified using a read-after-write configuration. The data recording density is 8000 bits per inch (bpi) using five flux transition positions to record four bits for a maximum of 10,000 flux transitions per inch (frpi). With a cartridge containing 450 feet of 1/4-inch magnetic recording tape, the total formatted data capacity is 45 megabytes (Mb).

The MCS consists of the following major components:

Mechanical Assembly Power Supply Main Drive Printed Circuit Board Formatter Printed Circuit Board

Two configurations may be encountered in the field. The early configuration, prior to the nine hundred thousand series model number shown in figure 1-2, differs from the later configuration, nine hundred thousand series model number and subsequent shown in figure 1-3, primarily in the power supplies used, the line filter used, and component locations as seen in the figures. The information in this manual applies to both configurations unless specifically noted otherwise. The major components are briefly described in the following paragraphs.

NOTE

The two PCBA's are mounted on the mechanical assembly. For most intents and purposes, the PCBA's and mechanical assembly can be treated as a single unit. For clarity in the system descriptions, the PCBA's and the mechanical assembly are discussed separately.





Figure 1-3. MCS Component Location, Later Configuration

1.1.1 Mechanical Assembly

The mechanical assembly contains the mechanical and drive drive components of the MCS. The entire assembly is housed within a die-cast aluminum substructure secured to the system lower chassis. Both the Main Drive and the Formatter PCBA's are mounted to the mechanical assembly. The component parts of the mechanical assembly are described in the following paragraphs.

1.1.1.1 Cartridge Loading and Seating Mechanism

The cartridge loading and seating mechanism accurately locks the cartridge in the optimum position relative to the magnetic head(s) by three registration point deck pins. A front-mounted lever is placed in the vertical position to secure the cartridge in the operating position. The aluminum substructure guides serve to maintain the close tolerances required for proper cartridge positioning.

1.1.1.2 Head Positioning Motor

A bidirectionally controlled, unipolar four-phase stepping motor performs head positioning functions. The motor is controlled by the microprocessor based driver circuit on the Main Drive PCBA.

1.1.1.3 Read/Write Head Assembly

The system utilizes a moveable read/write magnetic head assembly consisting of two read heads and two write heads. The two read heads permit bidirectional reading necessary for the serpentine recording format. The two write heads permit bidirectional writing in the serpentine format; one head records on even numbered tracks in the forward direction and the other records on odd numbered tracks in the reverse direction. An erase bar is mounted on the head assembly to produce a fvll-width AC erase field.

1.1.1.4 DC Capstan Motor

A three phase, brushless DC motor drives the tape in a streaming (continuous) mode of operation at a speed of 90 ips. The motor drives a 5/8-inch capstan and accelerates the tape to operating speed in 350ms. The motor speed is controlled by a tachometer signal derived from three Hall-Effect motion position sensors.

1.1.1.5 BOT/EOT Photosensing Assembly

Beginning-of-Tape (BOT) and End-of-Tape (EOT) sensing is accomplished by illuminating the tape with light emitting diodes (LED's) and recognizing the light through tape windows with two photo transistors.

1.1.2 Main Drive PCBA

The Main Drive PCBA is the basic interface between the drive mechanism and the Formatter PCBA and contains circuitry to perform the following functions:

- o Control the tape speed
- o Control head positioning
- o BOT/EOT sensing
- o Read, write, and erase signal processing
- o Supply 12 or 24 volts dc

1.1.3 Formatter PCBA

The Formatter PCBA contains independent read and write control circuitry, four 4K-bit data buffers, host interface circuitry, and a microprocessor to perform the following three major functions:

- o Recognize and format data written to or read from the tape
- o Multiplex a 16K x 1-bit memory into four 4K data buffers
- o Provide control and handshake signals to interface with the host

1.1.4 Power Supply

The MCS uses 5- and 12-volt power. Early system configurations have separate 5-volt and 12-volt power supplies attached by screws to the system chassis. Later system configurations have both power supplies mounted on a single board attached to the chassis by a bracket.

1.2 MODEL 4403 MCS SPECIFICATIONS

Table 1-1 lists the specifications for the Model 4403 Magnetic Cartridge Streamer.

Table 1-1. Model 4403 MCS Specifications

PARAMETERS	CHARACTERISTICS
PHYSICAL	
Height	3.38in (8.59cm)
Width	5.88in (14.94cm)
Depth	8.00in (20.32cm)
Weight	4.51bs (2.04kg)
Maximum Shipping Weight	10.001bs (4.54kg)

POWER

DC Voltage Control Logic	12 <u>+</u> 0.6V or 24 <u>+</u> 4. 5 <u>+</u> 0.25V	8V
Maximum P-P Ripple (included in tolerance)	+12V = 200mV +5V = 50mV	
	<u>+5</u> V	<u>+12</u> V
Standby Current	1.0A	200mA
Operating Current	2.2A	1.8A
Maximum Motor Startup Surge	2.6A for 350ms @ +12	2V
Power Dissipation	30W, 42W surge	

- -

Table 1-1. Model 4403 MCS	Specifications (continued)
PARAMETERS	CHARACTERISTICS
ENVIRONMENTAL	
Temperature Range Operating Nonoperating	+41° to +113°F (+5° to +45°C) -22° to +140°F (-30° to +60°C)
Relative Humidity Operating Nonoperating	20% to 80%, noncondensing 1% to 90%, noncondensing
Altitude Operating Nonoperating	Sea level to 10,000 feet (3km) Sea level to 49,000 feet (15km)
Temperature Gradient, Operating	1°C minute maximum
DATA HANDLING	
Capacity (formatted) 450-ft Tape	45 Mb
Recording Tracks	9
Density	8,000 bpi
Transfer Rates 90 ips Maximum Burst	86.7 kbits/sec 200 kbits/sec
Recording Form	9-track, serpentine, bidirectional
Data Buffering	3 x 512 bytes
Recording Code	(0,2) Run Length Limited
Head Type	2-channel read-after-write with full-width AC erase bar
Maximum Error Rate Soft Read Hard Read	1×10^{8} 1 x 10 ¹⁰
Mean Time Between Failures	20,000 hours with 20% workload

Table 1-1. Model 4403 MCS	Specifications (continued)		
PARAMETERS	CHARACTERISTICS		
DATA HANDLING (continued)			
Intelligent Interface Standard	QIC-02, rev. D		
Data Interchange Format	QIC-24, rev. D		
Gap Spacing Read to Write Write to Erase	0.30 inches 0.30 inches		
GENERAL			
Read/Write Speed	90ips		
Search/Erase Speed	90ips		
Tape Motion	Steady state , streamer operation		
Speed Variation Short Term Long Term	47% maximum +3% maximum		
Start/Stop Time	350ms		
Cartridge Specification	ANSI Standard X3.55-1977		
Signal Levels (to host) Logic High (0) Logic Low (1)	2.4 to 5.25VDC 0.0 to 0.55VDC		
Signal Levels (to MCS) Logic High (0) Logic Low (1)	2.0 to 5.25VDC 0.0 to 0.8VDC		
Interface Cable	50 conductor, flat ribbon, 3 meter maximum length		
Interface Connector	50-pin PWB edge connector, 3M type 3415-0001		

SECTION II

INSTALLATION

2.1 GENERAL

This section contains installation instructions for the system.

2.2 UNPACKING PROCEDURES

The Model 4403 MCS is thoroughly tested and carefully packed prior to shipping in accordance with industry standards. Refer to the following steps when unpacking the system.

- 1. Examine the shipping container for dents, cracks, or other evidence of shipping damage. Report any shipping damage to the Technical Support Representative immediately.
- 2. Open the shipping container and remove the system and any accessories. Examine the system and accessories for signs of concealed shipping damage. Verify component parts are not missing or lost per the shipping list. If any discrepancies or concealed shipping damage is discovered, notify the Technical Support Representative immediately.

2.3 PREINSTALLATION PROCEDURES

The following paragraphs describe the Preinstallation procedures.

2.3.1 AC Power Requirements

Verify the following:

- a. The AC power source to the MCS should be a dedicated line source. The AC line must not be shared by devices or equipment causing large transients (for example, air conditioners, heaters, or other equipment with large motors).
- b. The AC power source to the MCS must not be subject to voltage variations greater than 10% or frequency variations greater than 0.2%.
- c. The MCS must be connected to the proper AC power source (110V, 60Hz or 220V, 50Hz) as applicable.
- d. The MCS must be located for direct connection to the power outlet without the use of an extension cord.

2.3.2 Grounding Requirements

The MCS ac power line must include a third wire earth ground that meets or exceeds the requirements of the National Electrical Code. Perform the following procedure to verify the grounding requirements.



Only three-wire connectors and three-pronged plugs with the third wire connected to an earth ground are acceptable electrical connectors. Under no circumstances are two-wire connectors or plugs to be used, with or without connection to a conduit ground. Improper grounding can result in unstable equipment operation and safety hazards.

1. Using a commercial Ground Impedance Checker (such as EGOS Model 1020) and the proper twist-lock adapter, verify proper wire connection and a sufficiently low ground impedance (less than two ohms) to ensure safe and correct performance.

NOTE

Improper implementation of the earth ground through ground wire connection to a neutral wire at the wall outlet could yield satisfactory ground impedance test results but improper equipment operation or safety hazards. The ground wire should be properly connected to an earth ground at the power distribution panel. As necessary, verify proper earth ground connection by physical inspection with the electrician responsible for wiring installation.

- 2. Measure the voltage drop as follows:
 - a. Connect the equipment to the AC power source.
 - b. Place the rear panel POWER switch on.
 - c. Verify the circuit breaker is properly reset.
 - d. Connect a digital voltmeter set to 20VAC to measure the voltage drop either between the green and white wires at the wall outlet or between the equipment power distribution chassis and the end of the incoming line. The measured drop must be less than 1.8VAC.

If the values measured in steps one and two do not meet the specified requirements, request the customer to provide a suitable power source.

2.4 MCS INSTALLATION

The MCS is a self-contained peripheral assembly. It can be located on a table or bench within cable length of the host computer. The MCS should not be placed on the host computer mainframe. Refer to the following procedure when installing the MCS.

- 1. Position the MCS in a suitable location.
- 2. Connect the MCS to the host computer with the supplied cable.
- 3. Connect the MCS power cord to an AC power source (110/220V, 50/60Hz).
- 4. Place the rear panel POWER switch to on to supply operating power.
- 5. Perform preventive maintenance procedures as necessary (refer to Section IV).

SECTION III

FUNCTIONAL DESCRIPTION

3.1 GENERAL

This section contains the functional description of the Model 4403 Magnetic Cartridge Streamer on the following levels:

- Operational description of the various tasks performed by the system
- Interface description of the various signals, commands, and power interfaces between the MCS and the host
- Block diagram description of the various circuit groups and their interrelationship

3.2 OPERATIONAL DESCRIPTION

The Model 4403 MCS is a 5 1/4-inch form factor cartridge tape drive designed to back up small rigid disk drives. The MCS utilizes a 4 x 6-inch cartridge with 1/4-inch wide magnetic tape for nine track recording. The system includes two microprocessor controlled printed circuit boards, the Main PCB and the Formatter PCB. All the required electronics are included on these boards. Descriptions of the various system functions are provided in the following paragraphs.

3.2.1 Main Drive PCB

The following paragraphs describe the functions of the Main Drive PCBA.

3.2.1.1 Tape Speed Control

The speed of the tape drive motor is controlled by a tachometer derived from three Hall-Effect motor position sensors. These sensors are processed by a control Programmable Read Only Memory (PROM) and routed to a frequency to voltage converter. The resulting voltage is compared to a nominal value and the difference between the voltages is determined. The difference signal is compared to a sawtooth voltage to generate the motor control voltage.

3.2.1.2 Head Positioning

A four phase, unipolar stepper motor performs the head positioning task. Step and directional controls are obtained from the microprocessor controlled gate array circuit on the Formatter PCB. A glass and graphite linear bearing is used in the head positioning mechanism.

3.2.1.3 Read/Write/Erase Signal

The read, write, and erase control signals are obtained through the 34-pin interface with the Formatter PCB. Two read heads and two write heads enable bidirectional read/write operations. The dual head configuration permits the internal read-after-write check. The enabled write head (selected by the TRO signal) is supplied with +12V, regardless of the applied voltage.

3.2.1.4 BOT/EOT Sensing

The back of the tape is illuminated by LED's. Holes punched through the tape at the BOT and EOT positions permit this light to be sensed by two photo transistors, enabling the drive to take the appropriate action.

3.2.2 Formatter to Main Drive PCB Interface

A 34-pin I/O connector is used to interface the Formatter PCB with the Main Drive PCB. The connector pin assignments are described in table 3-1.

Table 3-1. Formatter to Main PCB Connector

PIN NUMBER	NAME	IN/OUT*	TRUE	DESCRIPTION
19	TRO	In	High	Track select bit 0
23	TR1	In	High	Track select bit 1
20	TR2	In	High	Track select bit 2
33	TR3	In	High	Track select bit 3
9	WDA-	In	* *	Inverse write data signal
10	WDA	In	* *	Write data signal
1	RST-	In	Low	Reset drive
29	WEN	In	High	Write enable control
25	EEN	In	High	Erase enable control
27	REV	In	High	Capstan servo direction control
31	GO	In	High	Capstan servo go control
7	KEY	-	-	Connector key
3	TACH-	Out	Low	Tachometer signal
2	LTH-	Out	Low	Lower tape position code
4	UTH-	Out	Low	Upper tape position code
5	USF-	Out	Low	Unsafe cartridge safe plug in unsafe
6	CIN	Out	Low	Cartridge in place
13	RDP	Out	Low	Read data pulse output
8,11,12,14,				
22,24,26,				
28,30,32	-	-	-	Connect to ground
15,16,17,				
18,21	-	_	-	Connect to 5 volts

* = Indicates in to or out from the Main PCB

3.2.3 Formatter PCBA

The Formatter PCB controls interfacing protocal, data block formatting, drive selection, reading status, tape retension, tape erasing, tape writing, and tape reading.

Host interfacing and data formatting are controlled by a microprocessor based, 48-pin CMOS gate array of 1500-gate complexity. The microprocessor decodes and interprets host command sequences for recording head reposition to the selected track, initiate tape movement, start the data through the gate array, and assemble and transfer MCS status signals. These functions are supported by the data formatter gate array that formats and recognizes data written to or read from the tape. The data formatter gate array multiplexes the 16K x 1-bit memory into four 4096 data buffers and provides control and handshake signals. The formatter gate array is controlled by the interface microprocessor through a bidirectional bus.

3.2.3.1 Tape Interface

The tape interface formats the data output from the buffer and block address memories for writing to the tape. During a read operation, the tape interface takes the data and block address from the tape input signal and stores them in the buffer and block address memories. During read and write operations, the data formatter performs the Cyclic Redundancy Check (CRC), generating and detecting as well as writing and detecting file marks.

3.2.3.2 Host Interface Control

The Formatter provides the host data transfer interface control. The Formatter provides the start signal (HCMP) and receives the completion signal (/Done) at the end of a single block transfer. The Formatter also provides a buffer memory, data input, data output, and strobe.

3.2.3.3 Microprocessor Interface

The Formatter interfaces with the control microprocessor through the processor data bus, three address lines, a select line, and the processor/write line. This interface utilizes standard peripheral protocol and timing.

3.3 RECORDING METHOD

The Model 4403 MCS uses the Non-Return-To-Zero (NRZ1) recording method. The NRZ1 method reduces the sensitivity to tape imperfections through lower density recording. The data encoding format is Group Code Recording (GCR), a Run Length Limited (RLL) code that uses five flux transition positions to record four bits. (Refer to paragraph 3.3.3 for a description of GCR encoding.)

3.3.1 Number and Use of Tracks

The MCS records on nine tracks in a serpentine fashion with even numbered tracks serially recorded in the forward direction and odd numbered tracks serially recorded in the reverse tape direction. The data is recorded in designated tape areas as shown and described in figure 3-1. Track numbering is also shown in figure 3-1. Tracks are recorded sequentially, 0, 1,. 2, ... 8.



8082-04

Figure 3-1. Track Numbering and Designated Areas

3.3.2 Data Block Format

The data block format, shown in figure 3-2, consists of a preamble, data block marker, data, block address, Cyclic Redundancy Check (CRC), and postamble.

3.3.2.1 Preamble

The preamble is used to synchronize the phase-lock loop in the read electronics with the data frequency. The preamble is also used to measure the average preamble amplitude. Three preamble lengths are possible when measured by a range of flux transitions recorded at the maximum nominal recording density of 10,000 flux transitions per inch (fti), described as follows:

- a. Normal The normal preamble length is 120 to 300 fti.
- b. Elongated The elongated preamble length is 3500 to 7000 fti and precedes the first data block recorded after an underrun sequence. (Refer to paragraph 3.3.5.4/5 for a description of an underrun sequence.)
- c. Long The long preamble length is 15,000 to 30,000 fti and precedes the first data block for interchange, recorded at the beginning of track 0.

3.3.2.2 Data Block Marker

The one byte data block marker is a unique byte identifying the end of the preamble and the start of the data block with the following CRC pattern:

G4	G3	G2	G1	GO	G4	G3	G2	Gl	GO

1 1 1 1 1 0 0 1 1 1

MS	nybble
----	--------

LS nibble



Figure 3-2. Data Block Format

3.3.2.3 Data Field

The data field is 512 bytes of host data encoded in the GCR format.

3.3.2.4 Block Address

BVTF

The block address, defined in table 3-2, is a unique four byte segment to identify the recorded data block. The address is encoded in the GCR format.

Table 3-2. Block Address Definition

BYTE	BITS	DEFINITION
0	0-7	Track number bits 0 (LSB) to 7 (MSB)
1	4-7	Control block bits 0 (LSB) to 3 (MSB). Control block value 0 identifies the current data block as user data or file mark. Control block value 1 identifies the current data block as control information. (Refer to Table 3-3 for the definition of control informa- tion.) Other control block values are reserved
1	0-3	Block address bits 16 to 19 (MSB)
2	0-7	Block address bits 8 to 15

3 0-7 Block address bits 0 (LSB) to 7

When the control block value equals 1, the current 512 byte data block contains control information. The control information is defined in table 3-3.

Table 3-3. Control Information Definition

DEEINTTON

BILF	DEFINITION
0	Drive type: 04H = 4 track, 09H = 9 track
1	Type of control block: OOH = none O1H = first block on the track O2H = last block on the track, terminates a completed track O3H = extended file marks
2	File mark number MSB
3	File mark number LSB
4 - OF	Reserved (set to 00H)
10 - 1FF	Not defined

3.3.2.5 Cyclic Redundancy Check (CRC)

A two byte CRC is used for error detection and is calculated over the 512 data bytes plus the four block address bytes. The CRC begins with an initial value of all ones and uses the following CRC generating polynomial:

$$X16 + X15 + x2 + 1$$

3.3.2.6 Postamble

The postamble is recorded following the CRC and has two possible lengths based on a range of flux transitions per inch recorded at the maximum nominal density of 10,000 fti, described as follows:

- a. Normal The normal postamble length is 5 to 20 fti and is recorded following the CRC as a guard band.
- b. Elongated The elongated postamble length is 3500 to 7000 fti and is recorded following an underrun sequence. (Refer to paragraph 3.3.5.4/5 for a description of an underrun sequence.)

3.3.2.7 Track Reference Burst

A track reference burst is recorded at the maximum nominal recording density of 10,000 fti between the BOT window and recorded data on track 0. The track reference burst starts between 0 and 15 inches from the BOT hole and must extend 3 to 4 inches past the load point hole.

3.3.3 GCR Data Encoding

To preclude the need for read circuits with complex data window functions, the 8-bit byte data in the NRZ1 code received from the host is converted to the GCR code. The data is reconverted during subsequent read operations. Logic ones are indicated by a flux reversal in the middle of the bit cell; zeros do not have a flux reversal. The GCR code converts four bit nybbles to five bit nybbles for a ten bit data stream with no more than two consecutive zeros. Table 3-4 illustrates 4-bit data to 5-bit GCR code conversion.

111132	4-BIT DATA	5-BIT GCR CODE
HEX	BINARY	BINARY
0	0000	11001
1	0001	11011
2	0010	10010
3	0011	10011
4	0100	11101
5	0101	10101
6	0110	10110
7	0111	10111
8	1000	11010
9	1001	01001
А	1010	01010
В	1011	01011
С	1100	11110
D	1101	01101
Е	1110	01110
F	1111	01111

Table 3-4. GCR Code

3.3.4 Repositioning Cycle

When a read or write operation is performed after a tape stop at any position other than the BOT or EOT window, the system must go through its repositioning cycle. If a write operation initiates the repositioning cycle such as could occur in a write buffer underrun, a gap of 0.3 inches will be written between the last data block and the new data block. The repositioning cycle is shown in figure 3-3.



Figure 3-3. Repositioning Cycle

3.3.5 Error Processing

The Formatter provides extensive error processing and recovery sequences to reduce the interface software effort to the Host. The following sections describe system error processing and recovery.

3.3.5.1 Read-After-Write Errors

Read-After-Write error processing and recovery is automatically performed by the Formatter. Three write command buffers are allocated in the following sequence to support the Read-After-Write check.

- a. Buffer one stores the data block currently being written, data block $\ensuremath{\mathrm{N+l}}$.
- b. Buffer two stores the data block currently being checked, data block $\ensuremath{\mathbb{N}}.$
- c. Buffer three stores the next data block transferred by the host.

The tape drive head assembly is designed with two gaps, one for writing and one for reading, separated by a distance of 0.3-inch. In tape streaming, the inter-record gap length is only 0.013-inch; therefore, the Formatter must begin writing the N+1 data block before the N data block is completely verified by the Read-After-Write check. If a CRC error is detected during the Read-After-Write check of data block N, the recovery sequence described below is initiated and repeated until either no CRC errors are detected or 16 consecutive rewrites of the same data block have occurred.

- a. The write channel finishes writing data block N+1.
- b. The write channel begins rewriting data block N.
- c. When (rewritten) data block N reaches the read head, read checking begins.
- d. The write channel finishes rewriting data block N.
- e. The write channel begins rewriting data block N+1.
- f. The read channel finishes reading (rewritten) data block N.

3.3.5.2 Read Errors

The read error recovery process involves rereading the Block-In-Error (BIE) 16 times before informing the host of an unrecoverable tape error. Rereading the BIE is referred to as a soft error retry. If an error is encountered during a read operation, the following sequence is initiated:

- a. Read the next data block.
- b. One of the following conditions will apply:
 - 1. The next data block contains no CRC error and has the same block address as the BIE, indicating the BIE was rewritten during the write operation. This is an expected condition invisible to the host. The read operation continues without informing the host of an unexpected condition.
 - 2. The next data block contains no CRC error and has a block address one greater than the BIE, indicating the BIE may or may not have been rewritten. This is also an expected condition invisible to the host. The read operation continues without informing the host of an unexpected condition.
 - 3. The next data block contains no CRC error and has a block address two or more greater than the BIE, indicating the BIE was not rewritten. This condition initiates the soft error retry sequence (beginning with the following step c).
- c. The tape is stopped.
- d. The tape is repositioned (as described in the reposition cycle, paragraph 3.3.4) and the read sequence continues.
- e. If the data block has not been recovered successfully within 16 retries, the Formatter transfers the BIE (if it can be located), informs the host of an unrecoverable read error, and terminates the read operation. A data block is always transferred unless:
 - 1. A read or write error abort occurs.
 - 2. No more data is recorded on the media.

If the data block transferred to the host is not the BIE, the host is alerted to this fact.

Soft error retries are invisible to the host. Consequently, a statistical counter is incremented for each soft error retry. The data is available to the host on demand. Data blocks with CRC errors that were rewritten during the write operation do not increment the soft error retry counter during a read operation.

3.3.5.3 Read Sequence Errors

Each data block written on the tape contains a block address byte. Data blocks rewritten due to a Read-After-Write error alter the normal sequence of blocks written on the tape. During a read operation, a block sequence error can be caused by a data block read from tape without a CRC error but with an unexpected address, that is, a block address error. A soft error retry sequence identical to the soft error retry sequence for a read error is initiated for a block address error.

3.3.5.4 Read Buffer Underruns

During a normal read operation, the Formatter locates the block of data, transfers it to the buffer memory (in the Formatter), and performs a CRC check. If no CRC errors are detected, the data block is transferred to the host. (If an error is detected, the read error sequence is initiated as described in paragraph 3.3.5.2.) The Formatter uses three buffer memories during the operation: one is allocated to the read channel, one is allocated to the host, and one is held in reserve in the event the host temporarily gets behind the read channel throughput.

A read buffer underrun occurs when the read channel has located the next data block and none of the three buffer memories are available. To avoid losing the data, a tape is stopped, a reposition sequence is initiated, and a normal read operation continues when a buffer memory becomes available. A statistical counter tracks the number of read buffer Underruns.

3.3.5.5 Write Buffer Underruns

A write buffer underrun occurs when the system is ready to write the next data block to the tape but the data is not available from the buffer memory. A last block sequence is initiated to rewrite the last data block available and the write buffer underrun counter is incremented.

If a new data block is available from the buffer memory before the read channel completes the Read-After-Write check of the rewritten data block, the write operation continues without a tape stop.

If a new data block block is still not available from the buffer memory upon completion of the Read-After-Write check of the rewritten data block, the last block sequence is completed and the tape is stopped. A write reposition cycle is initiated which will result in a 0.3-inch gap on the tape between data blocks. The data throughput decrease resulting from each write buffer underrun reduces total, tape capacity by 0.98-inch or 1.76 data blocks.

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3.5.6 No Data Detected Errors

e Formatter searches a length of tape equal to approximately 128 data blocks r a specific block on the read channel. If the specific block is not found, reposition cycle is performed and the search is repeated up to two times. If e specific block is still not found, the Formatter informs the host of an uncoverable error due to no data detected and does not transfer a data block.

3.4 INTERFACE DESCRIPTION

The following paragraphs describe the host/MCS interface characteristics.

3.4.1 Signal Interface

The signal interface is designed to minimize the number of interconnects between the host system and the MCS and is compatible with the standard QIC-02, rev. D. The signal interface is divided into three categories relative to the MCS: control input lines, control output lines, and data transfer lines. Data and commands are transferred to and from the MCS over an 8-bit bidirectional data bus using asynchronous techniques. Figure 3-4 illustrates the host to MCS signal interface. All signals to the host are TTL levels as follows:

> FALSE: Logic 0 (high) = 2.4 to 5.25VDC TRUE: Logic 1 (low) = 0.0 to 0.55VDC

All signals to the MCS are TTL levels as follows:

FALSE: Logic 0 (high) = 2.0 to 5.25VDC TRUE: Logic 1 (low) = 0.0 to 0.8VDC



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Figure 3-4. Host to MCS Signal Interface

3.4.2 Input/Output Signal Pin Assignments

The interface connection is through a 50-pin PWB edge connector. Pins are numbered 1-50, even numbers on the component side of the PWB, odd numbers connected to signal ground. The key slot is located between pins 4 and 6 to ensure proper cable connection. The recommended mating connector is a 3M type 3415-0001, 50-pin connector. The signal cable is a 50 conductor flat ribbon type. Input/output signal pin assignments and signal descriptions are provided in table 3-5.

Table 3-5. Input/Output Pin Assignments

PIN NUMBER	NAME	то	DESCRIPTION
02	SPR-	Х	Spare
04	SPR-	Х	Spare
06	SPR-	Х	Spare
08	SPR-	Х	Spare
10	HBP-	В	Host bus odd parity - optional
12	HB7-	В	Host bus bit 7 - MSB on 8-bit bidirectional data bus
14	НВ6-	В	Host bus bit 6
16	HB5-	В	Host bus bit 5
18	HB4-	В	Host bus bit 4
20	HB3-	В	Host bus bit 3
22	HB2-	В	Host bus bit 2
24	HB1-	В	Host bus bit 1
26	HBO-	В	Host bus bit 0 - LSB on 8-bit bidirectional data bus
28	ONL-	М	ON LINE signal activated by the host prior to transferring a read or write command and deacti- vated by the host to terminate a read or write command
30	REQ-	М	REQUEST signal activated by the host to indicate command data has been placed on the bus in the command mode or status data has been taken from the bus in the status input mode. The REQUEST signal can only be activated by the host when either RDY- or EXC- is activated by the MCS
32	RST-	М	RESET signal activated by the host to initialize the MCS with a default selection of drive 0 and causing the MCS to assert the EXC- signal
34	XFR-	М	TRANSFER signal generated by the host to indicate data has been placed on the bus in the write mode or data has been taken from the bus in the read mode
36	ACK-	Η	ACKNOWLEDGE signal generated by the MCS to indi- cate data has been taken from the bus in the write mode or data has been placed on the bus in the read mode

^_

	Table	3-5.	Input/Output Pin Assignments (continued)
PIN NUMBER	NAME	ТО	DESCRIPTION
38	RDY-	Н	READY signal generated by the MCS to indicate one of the following conditions:
			a. Data has been taken from the bus in the com- mand transfer mode
			b. Data has been placed on the bus in the status input mode
			c. A BOT, retension, or erase has been completed
			d. A buffer is ready to be filled by the host or a Write File Mark (WFM) command can be issued in the write mode
			e. A WFM command is completed in the write file mark mode
			f. A buffer is ready to be emptied by the host in the read mode
			g. The MCS is ready to receive a new command
40	EXC-	Н	EXCEPTION signal generated by the MCS to indicate an exception condition exists in the Formatter. The host must issue a status command and perform a status input to determine the cause of the ex- ception
42	DIR-	Н	DIRECTION signal generated by the MCS. When false, the host data bus drivers assert their data bus levels and the MCS data bus drivers assume a high impedance state. When true, the MCS data bus drivers assert their data bus levels and the host data bus drivers assume a high impedance state
44	SPR-	Х	Spare
46	SPR-	Х	Spare
48	SPR-	Х	Spare
50	SPR-	Х	Spare

"TO" nomenclature:

- X = undefined
- B = bidirectional
- H = host
- M = MCS

All odd number pins are signal returns connected to signal ground.

3.4.3 Signal Termination

Signal termination used is 220 ohms to +5VDC and 330 ohms to ground or the Thevenin equivalent. Resistance tolerance is +5% maximum. The bidirectional data bus and the four control lines from the host are terminated at the MCS unless two or more devices are daisy chained together, in which case the lines are terminated at the last device in the chain. The four control lines and the bidirectional data bus from the MCS are terminated at the host.

3.4.4 Signal Loading

Signals on the interface, either loaded by the host or by the MCS, shall not be more than 2.0mA plus the current required for termination.

3.4.5 Control Output Signals

The four control output signals from the MCS to the host are READY, EXCEPTION, ACKNOWLEDGE, and DIRECTION. These signals are further described in the following paragraphs.

3.4.5.1 READY Control Output

READY (RDY) is used to indicate one of the following conditions, depending on the operation being performed.

- a. If no operation is currently being performed, READY indicates the MCS is prepared to accept a new command.
- b. During a command transfer, READY going true indicates to the host that the MCS has taken the command from the data bus.
- c. During a status byte transfer from the MCS to the host, READY going true indicates the next status byte is available on the data bus.
- d. At the conclusion of a tape positioning command from the host, READY going true indicates the operation has been completed.
- e. During a write operation, READY going true indicates a buffer is available to be filled by the host or a WFM command can be issued.
- f. At the conclusion of a WFM command from the host, READY going true indicates the operation has been completed.
- g. During a read operation, READY going true indicates a buffer is ready to be emptied by the host.

3.4.5.2 EXCEPTION Control Output

EXCEPTION (EXC) is set true to indicate to the host that the execution of a command has been terminated. The only response to EXCEPTION going true is for the host to issue a Read Status command. The MCS will set EXCEPTION true for the following conditions:

- a. When an error condition is detected, or
- b. When the MCS reads a file mark, or
- c. When the MCS receives the RESET signal either from the host or as a result of a power-up condition. (Any time the power is applied to the MCS, the first command it must receive is a Read Status command.)

3.4.5.3 ACKNOWLEDGE Control Output

ACKNOWLEDGE (ACK) is used by the MCS during data transfer operations. During a write operation, ACKNOWLEDGE is set true to indicate the MCS has received the data from the host. During a read operation, ACKNOWLEDGE is set true to indicate the data from the MCS is available to the host.

3.4.5.4 DIRECTION Control Output

DIRECTION (DIR) is used by the MCS to indicate the direction of data flow across the data bus. DIRECTION is set true to indicate data transfer from the MCS to the host and is set false for data transfers from the host to the MCS. Normally, DIRECTION is false and only goes true for a status byte transfer or a read operation.

3.4.6 Control Input Signals

The four control input signals from the host to the MCS are ON LINE, REQUEST, TRANSFER, and RESET. These signals are further described in the following paragraphs.

3.4.6.1 REQUEST Control Input

The host sets REQUEST (REQ) true to indicate a command is ready to transfer to the MCS. REQUEST is also used to indicate a status byte has been taken from the data bus.
3.4.6.2 ON LINE Control Input

The host sets ON LINE (ONL) true before placing a Read, Write, RFM, or WFM command on the data bus and before setting REQUEST. The host can also use ON LINE to terminate a read or write operation by resetting it to false. When the MCS detects ON LINE going false during a write operation, it finishes writing to the tape the data remaining in the buffers, writes a file mark, and rewinds the tape to the BOT window. If the host issued a WFM command prior to resetting ON LINE to false, the MCS will not write another file mark. If the MCS detects ON LINE going to false during a read operation, the data transfer is stopped at the next block boundry even if other data blocks remain in the buffers. When the transfer is stopped, the tape is rewound to the BOT window.

3.4.6.3 TRANSFER Control Input

TRANSFER (XFER) is used by the host during transfer operations. During a write operation, TRANSFER is set true by the host to indicate data is available to the MCS. During a read operation, TRANSFER is set true by the host to indicate the host has read the data from the data bus.

3.4.6.4 RESET Control Input

RESET (RST) is a direct line to the MCS reset circuitry and performs the same function as a power-on reset.

3.4.7 Command Signals

All commands are single, 8-bit byte commands. The three most significant bits (bits 7,6,and 5) define the type of command; the five least significant bits (bits 4 through 0) contain the command data. The seven possible command types are identified in table 3-6 and individually described in the following paragraphs.

Table 3-6. Command Types

COMMAND TYPES	MSB (Bits 7,6,5)	LSB (Bits 4-0)
Select	000	MMMMM
Position Write Data	001 010	OOMMM 00000
Write File Mark (WFM)	011	00000
Read Data	100	00000
Read File Mark (RFM) Read Status	101 110	00000 00000

The MCS will only accept a command from the host when the READY signal is true except for the Read Status command. The MCS will accept the Read Status command if the EXCEPTION signal is true. Read Status is the only command accepted when EXCEPTION is true. The MCS requires ON LINE to be true in addition to READY being true for the following four commands:

- a. Write Data
- b. Write File Mark
- c. Read Data
- d. Read File Mark

The MCS sets EXCEPTION if the host issues one of these commands without ON LINE being true. The other commands do not require or care if ON LINE is set.

3.4.7.1 Read Status Command

The Read Status command is used to either read the drive status or run the self test and read the self test status. The Read Status command sequence proceeds as follows.

- a. The host places the Read Status command on the bus after sensing the EXCEPTION signal is true.
- b. After the command is on the bus, the host sets REQUEST to inform the MCS a command is present.
- c. The MCS resets EXCEPTION after sensing REQUEST.
- d. The MCS sets READY to inform the host the command has been read off the bus.
- e. The host resets REQUEST after sensing READY is true and the command can be removed from the bus.
- f. The MCS resets READY after REQUEST goes false.
- g. The MCS sets DIR true to change direction of the bus in preparation for sending the first status byte.
- h. The MCS places the first status byte on the data bus.
- i. The MCS sets READY true to begin handshaking the status bytes to the host.
- j. The host reads the status byte from the bus after sensing READY and sets REQUEST to inform the MCS the data has been read. When REQUEST is set, the data on the bus becomes invalid.

- k. The MCS will reset READY in response to the host confirmation.
- 1. The host resets REQUEST in response to a reset READY to complete transmission of the first status byte. The MCS places the next status byte on the bus and the transmission process is repeated, beginning with step i, until the last status byte has been transmitted.
- m. After the host resets REQUEST for the last status byte (step 1), the MCS will reset DIR and the host will wait for READY to begin the next operation.

If the Read Status command occurs at the end of a read or write sequence, the sequence is as follows:

- a. The host places the Read Status command on the bus after sensing the READY signal is true.
- b. After the command is on the bus, the host sets REQUEST to inform the MCS that a command is on the bus.
- c. The MCS responds by resetting READY when REQUEST is true.
- d. After reading the command from the bus, the MCS will again set READY to inform the host that the command has been read.
- e. The rest of the sequence is the same as in response to EXCEPTION, described in steps e through m above.

The timing sequence for the Read Status command used to run and read the self test has not been determined.

3.4.7.2 Select Command

The Select Command is used to select one of four drives if multiple drives are used with the host system. If the Select Command is not issued after the power up reset (and after the Read Status command), drive 0 is selected by default. The least significant bits of the Select command are used for drive selection as shown in table 3-7.

Table 3-7. Select Command

SELECT	MSB (BITS 7-5)	LSB (BITS 4-0)
*	000	10000
Drive 3	000	01000
Drive 2	000	00100
Drive 1	000	00010
Drive O	000	00001

* = Select Light Bit (see following text)

Bits 0 through 3 are used to select the drive. Bit 4, the Select Light bit, is used as a logical cartridge lock. When a Select command is issued with bit 4 not set, the select light will go off at the conclusion of an operation when the tape is at the BOT window, track 0. When a select command is issued with bit 4 set, the select lamp will remain lit between operations to inform system users that the drive is in use and the cartridge should not be removed. If the cartridge is removed when the select lamp is lit, the EXCEPTION signal will go true and the status byte will indicate cartridge not in place.

If a Select command is issued which selects two drives simultaneously or does not select any drive, the EXCEPTION signal will go true and the status byte will indicate an illegal command.

The Select command sequence proceeds as follows:

- a. The host places the Select command on the bus after detecting the READY signal is true.
- b. The host sets REQUEST to inform the MCS the command is on the bus.
- c. The MCS responds to REQUEST by resetting READY. The host will keep the command on the bus and keep REQUEST true.
- d. When the MCS has read the command from the bus, it will set READY true to inform the host that the command has been accepted.
- e. When the host detects READY going true, it will reset REQUEST and the command can be removed from the bus.
- f. The MCS will reset READY when REQUEST is reset.
- g. After some period of time, the MCS sets READY true again to inform the host the command has been performed and the next operation can begin.

3.4.7.3 Position Command

The Position command is used to rewind, retension, or erase the tape. The command function is selected by the least significant bits as shown in table 3-8. All Position command functions are performed at a tape speed of 90 ips.

Table 3-8. Position Command

FUNCTION	MSB (BITS 7-5)	LSB (BITS 4-0)
Degenerad	0.01	10000
Reserved	001	10000
Reserved	001	01000
Retension	001	00100
Erase Tape	001	00010
Rewind to BOT	001	00001

The rewind function permits the host to position the tape before performing a read or write operation. If the rewind instruction is not preceded by a Select command, drive 0 will be selected automatically. Upon receiving the rewind instruction, The MCS checks for proper cartridge insertion. If a cartridge is not fully inserted, the command is aborted and the EXCEPTION signal is set. If no abnormal conditions are detected after performing the rewind instruction, READY will be set. If a Position command is not issued prior to a Read, Write, WFM, or RFM command, the MCS will automatically position the tape at the BOT window.

The erase function is used to completely erase the cartridge. The erase function causes the tape to be rewound to the BOT window, erased completely from BOT to EOT, and then repositioned at the BOT window. During a normal write operation, the erase head is activated to erase the full tape width directly ahead of the write head. However, if a new data file written to the tape is not as long as track zero, as in multiple WFM commands to determine the number of files on tape, old data may remain on the tape.

The retension function performs a retensioning pass as recommended by cartridge tape manufacturers. In a retensioning pass, the tape is positioned at the BOT window, moved from the BOT to the EOT, and then rewound to the BOT window. The repositioning pass is best used prior to a write operation, when excessive read errors are detected, or prior to reading for hard tape errors.

The Position command sequence proceeds as follows:

- a. The host places the Position command on the bus after sensing READY is true.
- b. The host sets REQUEST to inform the MCS the command is on the bus.
- c. The MCS responds to REQUEST by resetting READY. The host will keep the command on the bus and keep REQUEST true.
- d. When the MCS has read the command from the bus, it will set READY true to inform the host that the command has been accepted.
- e. When the host detects READY going true, it will reset REQUEST and the command can be removed from the bus.
- f. The MCS will reset READY when REQUEST is reset.
- g. After resetting READY, the MCS will perform the Position command, which could require as much as three minutes for the mechanical operation. At the end of the positioning operation, the MCS will again set READY true to inform the host the command has been performed and the next operation can begin.

3.4.7.4 Write Data Command

The Write Data command is used to write user data blocks to the tape. If a write operation is not preceded by a Select or Position command, drive 0 will be selected and the tape will be positioned at the BOT window, track 0 automatically. The host must set ON LINE true before issuing the Write Data command. If ON LINE is not true before the Write Data command, the MCS will respond with EXCEPTION and the status byte will indicate an illegal command.

Upon receipt of a Write Data command, the MCS checks for proper cartridge insertion and if the cartridge is write protected. If either condition prevents writing to the tape, the MCS will set the EXCEPTION signal. The write operation will continue until terminated by the host, either by resetting ON LINE or by issuing a WFM command after transmitting the last data block, or until terminated by the MCS in the event of a hard data error.

If the Write Data command is terminated by a WFM command, the MCS stops accepting new data from the host, finishes writing and read checking the data remaining in the buffers, and writes and read checks the file mark. Following the WFM, the host can resume writing by issuing another Write Data command, issue another WFM command, or rewind the tape to the BOT window by issuing a Position command or by resetting ON LINE.

If the Write Data command is terminated by the host resetting ON LINE, the MCS will finish writing and read checking the data in the buffers, write and read check a file mark, and rewind the tape to the BOT window.

If the Early Warning Hole (EWH) of the last track is detected during the write operation, the MCS stops accepting data from the host on a 512 byte block boundary, writes and read checks the data remaining in the buffers, stops tape motion, and sets EXCEPTION. The host must respond with a Read Status command. The status bytes will inform the host of the End of Media (EOM) status. When the EOM is reached, the host can respond by issuing a Write Data command, issuing a WFM command, or resetting ON LINE.

If a Write Data command is issued in response to the EOM, the MCS will accept two data blocks and repeat the EOM procedure. The host should use the two data blocks to note the file, if incomplete, is continued on another cartridge. A file mark should be written following the two data blocks to indicate all data was recovered when the file is read.

If a Write Data command is issued in response to the EOM but no data is transferred and ON LINE is then reset, a file mark will be written and the tape will be rewound to the BOT window.

If ON LINE is reset in response to the EOM without a Write Data or WFM command, the tape is rewound to the BOT window and no file mark is written. Again, a file mark should be written to ensure the host is aware that all the data was recovered when the file is read.

The Write Data command sequence proceeds as follows:

- a. The host places the Write Data command on the bus after sensing READY is true.
- b. After the command is on the bus, the host sets ON LINE and subsequently sets REQUEST to inform the MCS the command is on the bus.
- c. The MCS responds to REQUEST by resetting READY. The host will keep the command on the bus and keep REQUEST true.
- d. When the MCS has read the command from the bus, it will set READY true to inform the host that the command has been accepted.
- e. When the host detects READY going true, it will reset REQUEST and the command can be removed from the bus.
- f. The MCS will reset READY when REQUEST is reset in preparation of accepting and writing the data.
- g. The MCS sets READY true to inform the host that it is ready for the first data block. The MCS will wait indefinitely for the first byte.
- h. The host should place the first byte on the bus and set XFER to inform the MCS the byte is on the bus. (Actually, XFER may be set up to 40ns prior to having the data on the bus.)
- i. After detecting XFER going true, the MCS will reset READY to begin the data transfer, byte by byte, using ACK - XFER handshake. READY remains false throughout the transfer of all 512 bytes.
- j. After reading the byte of data from the bus, the MCS will set ACK to inform the host the data has been received.
- k. In response to ACK going true, the host resets XFER and the data can be removed from the bus.
- 1. When the MCS detects XFER going false, it resets ACK to complete the handshake of the first data byte.
- m. The XFER ACK handshake cycles 512 times. The MCS counts the number of data bytes transferred and at the conclusion of the transfer of byte number 512, ACK is reset to complete the handshake of the last byte.
- n. After ACK was reset for the last byte, the MCS sets READY to inform the host it is ready for the next data block.
- o. When the host detects READY going true, it begins the transfer of the first byte of the next data block. The MCS knows the bus contains data because REQUEST has remained false.

- p. The host can terminate the write operation by issuing a WFM command or by resetting ON LINE. When the MCS detects ON LINE false after setting READY at the last data block, the MCS will terminate the write operation, reset READY, write and read check a file mark, and rewind the tape to the BOT window.
- q. When the tape is in position at the BOT window, the MCS will set READY true to inform the host the command has been performed and the next operation can begin.

3.4.7.5 Write File Mark Command

The WFM command is used to instruct the MCS to write a file mark (or to write a file mark on the fly). The WFM has Oil in the MSB position (bits 7-5) and all zeros in the LSB position (bits 4-0). (If one of the LSB bits are set, the command is a WFM on the fly command, described in paragraph 3.4.7.6) File marks can be used to separate the data stored on tape into smaller segments along physical divisions, for example disk tracks and cylinders, or along logical divisions, for example data files.

A file mark is a full block of data. The host issues the WFM command, but does not transfer a block of data. Consequently, the MCS creates and writes 512 bytes of a unique code that cannot appear in a user data field.

When the host issues a WFM command, the ON LINE signal must be true. During a write operation, a WFM command can only be issued between data block transfers, not while a data block is being transferred. (During a data block transfer, the READY signal is false which inhibits the MCS from accepting a new command.) When a WFM command is issued during a write operation, the write operation is terminated (see the Write Data command description, paragraph 3.4.7.4), the file mark is written, and if ON LINE is held true, the tape is not rewound.

The WFM command sequence proceeds as follows:

- a. The host places the WFM command on the bus after sensing READY is true.
- b. After the command is on the bus, the host sets ON LINE and subsequently sets REQUEST to inform the MCS the command is on the bus.
- c. The MCS responds to REQUEST by resetting READY. The host will keep the command on the bus and keep REQUEST true.
- d. When the MCS has read the command from the bus, it will set READY true to inform the host that the command has been accepted.
- e. When the host detects READY going true, it will reset REQUEST and the command can be removed from the bus.
- f. The MCS will reset READY when REQUEST is reset and perform the command (write the file mark).

- g. After writing the file mark, the MCS will set READY true. The host should be monitoring the READY signal.
- h. When the host detects READY going true, ON LINE can be reset. (If the last command was a WFM, the MCS will not write another file mark when ON LINE is reset.)
- i. In response to ON LINE going false, the MCS will reset READY and rewind the tape to the BOT window.
- j. When the tape is in position at the BOT window, the MCS will set READY true to inform the host the command has been performed and the next operation can begin.

3.4.7.6 Write File Mark On The Fly Command

The WFM on the fly command (an optional command) has 011 in the MSB position (bits 7-5) and one bit set in the LSB position (bits 4-0). It is a combination of a WFM command and a Write Data command. When this command is received, the MCS finishes writing and read checking the data in the buffers and then writes a file mark in the same manner as a standard WFM command. While the file mark is being written, the MCS sets READY true to inform the host it is ready for a data transfer. The host should transfer a block of data in the time required to write the file mark (approximately 5ms at 90ips) to maintain streaming. The MCS proceeds with writing the block of data and continues with a normal write operation. If the data block is not available to the MCS in time, a write underrun will occur. The ON LINE signal must be true before the WFM on the fly command is issued.

During the execution of the WFM on the fly command, the MCS enters into the normal write mode of operation after the file mark has been written. Consequently, the only legitimate commands that the host can issue to the MCS are:

- a. Write File Mark on the fly
- b. Write File Mark
- c. Write Data
- d. Write Residual Block (optional)

The host could also reset ON LINE to terminate the write operation.

3.4.7.7 Read Command

The Read command is used to read user data from the tape. The Read command has 100 in the MSB position (bits 7-5) and all zeros in the LSB position (bits 4-0). (If one of the LSB bits are set, the command is a Continuous Read command, described in paragraph 3.4.7.8) If a Select command is not issued prior to a Read command, device 0 is selected automatically.

If a position command is not issued prior to a Read command, the MCS automatically positions the tape at the BOT window. The host must also set the ON LINE signal prior to issuing a Read Command or the MCS will respond with EXCEPTION.

When the MCS receives the Read command, it checks for proper cartridge insertion. If not properly inserted, the MCS aborts the operation.

The MCS will terminate a read operation after reading a file mark or after transferring a Block-in-Error (BIE) when an unrecoverable read error occurs upon detecting an erased tape.

To continue reading the next file after a file mark or the next data block after a BIE, the host must maintain ON LINE true and issue another read command. (If the BIE was a file mark, the next block of data will be the first block of the next file.) To terminate a read operation, the host can reset ON LINE. When ON LINE is reset, the MCS will terminate the read operation and rewind the tape to the BOT window, track 0. If ON LINE remains true after the read operation is terminated by the MCS, the tape can be rewound to the BOT window with a Position command.

During a read operation, a RFM command is the only legal command that can be issued. It is used by the host to relieve data handling responsibilities when searching for a specific file. If the first few data blocks of a file have been read and it has been determined that the required data is not contained in that file, a RFM command from the host will cause the MCS to read to the next file mark without transferring more data.

The Read command sequence proceeds as follows:

- a. The host places the Read command on the bus after sensing READY is true.
- b. After the command is on the bus, the host sets ON LINE and subsequently sets REQUEST to inform the MCS the command is on the bus.
- c. The MCS responds to REQUEST by resetting READY. The host will keep the command on the bus and keep REQUEST true.
- d. When the MCS has read the command from the bus, it will set READY true to inform the host that the command has been accepted.
- e. When the host detects READY going true, it will reset REQUEST and the command can be removed from the bus.
- f. The MCS will reset READY when REQUEST is reset in preparation of reading and transferring the data.
- g. The MCS will set DIRC true to change direction of the bus. The host should monitor READY to begin the data transfer.
- h. The MCS will set READY to inform the host the first data block is ready.

- i. The MCS will place the first byte of the first data block on the bus and simultaneously set ACK true. (The READY signal going true, step h, can lag behind the ACK signal going true.)
- j. The host detects ACK going true, reads the data from the bus, and sets XFER true to inform the MCS the data has been received.
- k. After the host sets XFER for the first byte of a data block, the MCS will reset READY. READY will remain false until the entire lock of data has been transferred and the next data block is ready. In addition, the MCS will reset ACK in response to XFER going true.
- 1. In response to ACK going false, the host will reset XFER in preparation for the next byte. This completes the ACK - XFER handshake.
- m. After XFER goes false, the MCS places the next data byte on the bus and sets ACK true to inform the host.
- n. The ACK XFER handshake is continued until 512 bytes have been transferred from the MCS to the host.
- o. After the host sets XFER true when the last byte of the block has been transferred, the MCS will set READY true to indicate the next data block is available.
- p. The entire handshake procedure is then repeated for this block and all subsequent blocks.
- q. In response to XFER going false to conclude the transfer of the last byte of the last block, the MCS will read a file mark.
- r. When the file mark is read, the MCS will reset DIRC to change the direction of the bus, set EXCEPTION, and stop tape motion.
- s. The only legal response to EXCEPTION from the host is to issue a Read Status command.

3.4.7.8 Read Continuous Command

The Read Continuous command has 100 in the MSB position (bits 7-5) and one bit set in the LSB position (bits 4-0). The Read Continuous command is identical to a Read Command except tape motion will not stop automatically when a file mark is detected. When a file mark is detected during a continuous read operation, the MCS will begin reading the next block and at the same time, the host will be alerted by EXCEPTION going true. The host must respond by reading the status bytes and issuing a new Read Continuous or Read command in the time required to read the next block (approximately 5ms at 90ips). If the host is unable to read the status and issue a new Read Continuous or Read command in the one block time frame, the MCS will perform a normal read underrun sequence.

3.4.7.9 Read File Mark Command

The RFM command is the same as a Read Command except no data is transferred to the host. At each file mark, the MCS sets EXCEPTION true to inform the host that a file mark has been found. If the host is looking for a particular file, it must count the number of file marks found and reissue RFM after each file mark.

The RFM command sequence proceeds as follows:

- a. The host places the Read command on the bus after sensing READY is true.
- b. After the command is on the bus, the host sets ON LINE and subsequently sets REQUEST to inform the MCS the command is on the bus.
- c. The MCS responds to REQUEST by resetting READY. The host will keep the command on the bus and keep REQUEST true.
- d. When the MCS has read the command from the bus, it will set READY true to inform the host that the command has been accepted.
- e. When the host detects READY going true, it will reset REQUEST and the command can be removed from the bus.
- f. The MCS will reset READY when REQUEST is reset and perform the command.
- g. The MCS reads the tape until a file mark is detected. When a file mark is read, the MCS will stop tape motion and set EXCEPTION. The status bytes will inform the host a file mark was read.

3.4.8 Status Bytes

Six status bytes are maintained by the MCS for use in informing the host of various conditions. The host may request the status bytes at any time by issuing a Read Status command. Status bytes 0 and 1 define the condition that caused the MCS to set EXCEPTION true. In both bytes, the MSB (bit 7) will be set if any other bit is set. If bit 7 is not set, no other bit should be set. Bytes 2 and 3 indicate the number of blocks rewritten during write operations and the number of soft read errors during read operations. Bytes 4 and 5 indicate the number of write Underruns during write operations and the number of read operations. The following paragraphs describe the status bytes.

3.4.8.1 Status Byte 0

Status byte 0 indicates certain conditions that may have caused the MCS to set the EXCEPTION signal. These conditions are described in table 3-9.

Table 3-9. Status Byte 0

BIT	CONDITION	DESCRIPTION
7	STO	Status Byte 0. This bit is set only if another bit in this byte is set.
б	CNI	Cartridge Not In Place. This bit is set if the car- tridge is not fully inserted in the drive.
5	USL	Drive Unselected. This bit is set if the selected drive is not physically connected or is not receiving power.
4	WRP	Write Protect. This bit is set if the cartridge write protect plug is set in the protect (safe) position.
		Bits 6-4 are dependent on the drive selected. The op- erator must correct the error condition before these status bits will reset.
3	EOM	End Of Media. This bit is set when the logical early warning hole of the last track is detected during a write operation. The bit will remain set as long as the drive is at its logical EOM. The bit will reset after the Read Status command.
2	UDA	Unrecoverable Data Error. This bit is set when the MCS experiences a hard error during read or write opera- tions. (After 16 retries to read or write a block of data, a hard error is detected, this bit is set, and the tape is rewound to the BOT window.) The bit is re- set after the Read Status command.
1	BNL	Block in Error Not Located. This bit is set when an

- unrecoverable read error occurs and the MCS cannot confirm that the last block transferred was the block in error. This bit will reset after the Read Status command.
- 0 FIL File Mark Detected. This bit is set when a file mark is read during a Read or a RFM command. This bit will reset after the Read Status command.

3.4.8.2 Status Byte 1

Status byte 1 indicates certain conditions that may have caused the MCS to set the EXCEPTION signal. These conditions are described in table 3-10.

Table 3-10. Status Byte 1

BIT	CONDITION	DESCRIPTION	
7	ST1	Status Byte 1. This bit is set only if another bit in this byte is set.	
6	ILL	Illogical Command. This bit is set if any of the fol- lowing conditions occur:	
		a. The Select command is issued with no drive se- lected or more than one drive selected (refer to paragraph 3.4.7.2).	
		 b. The Position command is issued with no qualifier bits set defining the command (refer to paragraph 3.4.7.3). 	
		c. The ON LINE signal is not asserted and a Write, WFM, Read, or RFM command is issued.	
		d. A command other than a Write or WFM command is issued during a write operation.	
		e. A command other than a Read or RFM command is issued during a read operation.	
		f. The drive is deselected when the cartridge is not positioned at the BOT window, track 0.	
		g. Any unimplemented command is issued.	
		This bit will reset after the Read Status command.	
5	NDT	No Data Detected. This bit is set when a unrecoverable data error occurred due to a lack of recorded data. Absence of recorded data is the failure to detect a data block within the time out period (32 block times). This bit will reset after the Read Status command.	
4	MBD	Marginal Block Detected. This bit is set when the MCS determines a data block is marginal (badly worn tape). This bit will reset after the Read Status command.	

Table 3-10. Status Byte 1 (continued)

BIT CONDITION DESCRIPTION

- 3 BOM Beginning of Media. This bit is set whenever the tape is logically at the BOT window, track 0. The bit will only reset as the tape moves away from the BOT window, not after a Read Status command. This bit alone will not cause EXCEPTION to go true.
- 2 RES Reserved.
- 1 RES Reserved.
- 0 POR Power On/Reset. This bit is set after the MCS receives a reset signal from the host or when power is applied. This bit will reset after the Read Status command.

3.4.8.3 Status Bytes 2 and 3

Status bytes 2 and 3 contain a 16-bit binary count of tape data errors. Byte 2 contains the MSB and byte 3 contains the LSB. During write operations, the count is incremented for each data block rewritten due to a read-after-write error. The rewrite sequence actually rewrites two data blocks for each error which will in turn increment the counter twice for each error. During Read operations, the count is incremented for each read retry. A read retry occurs whenever a CRC error occurs during a write sequence and is corrected by writing a second iteration of the block.

3.4.8.4 Status Bytes 4 and 5

Status bytes 4 and 5 contain a 16-bit binary count of buffer Underruns. Byte 4 contains the MSB and byte 5 contains the LSB. The count is incremented during a write operation for each write buffer underrun (refer to paragraph 3.3.5.5). The count is incremented during a read operation for each read buffer underrun (refer to paragraph 3.3.5.4).

3.5 BLOCK DIAGRAM DESCRIPTION

The MCS contains the Main Drive and the Formatter PCBA's, both mounted on the cassette drive mechanical assembly. The following paragraphs provide a block diagram description for the electronics on each of these boards.

3.5.1 Main Drive PCBA

The block diagram shown in figure 3-5 illustrates the tape speed control, head positioning control, BOT/EOT sensing, and read/write/erase signal processing functions of the Main Drive PCBA.



Figure 3-5. Main Drive PCBA Block Diagram

3.5.1.1 Tape Speed Control

Signals DMPA, DMPB, and DMPC at connector J7 pins 1, 2, and 3 respectively are leads to the motor windings from switches U30, U29, and U28. Two of these switches are active at any given time to provide current and polarity to the motor for proper motor rotation. Three Hall-Effect sensors detect the magnetic field in the motor to provide flux pattern information for tachometer feedback. The time relationship of the flux pattern activity provides the raw data input for motor speed control.

Input to the switches comes from the ROM U23. The ROM utilizes the Hall-Effect sensor data, the FOR- signal, and the INH signal to activate the appropriate switches for proper motor rotation. The FOR- signal is the motor direction signal supplied by the Main Drive board gate array processor U12. The INK signal activates the ROM; INK is generated by MON-, motor on, also from the Main Drive board gate array processor.

The comparator U26 will trip if the voltage exceeds three amps to inhibit the motor. The motor is inhibited for a 10µs shut down via the ILIM signal deactivating the INH signal to the ROM.

The three Hall-Effect feedback signals to the ROM are output as RTK to the tachometer pulse generator circuit. Two one-shot flip-flops produce the PTACH signal at approximately twelve pulses per motor revolution. PTACH goes to the Formatter board and to the Main Drive board gate array processor. If the gate array processor does not detect PTACH, it shuts down the motor with MON-. PTACH and PREF provide a voltage proportional to speed via a frequency to voltage converter that is compared to a sawtooth signal at U22 to give PWD, pulse width disable. The pulse width modulation compared to the sawtooth signal affects the INH signal to the ROM for the tape speed control.

Test Point eight can be used to verify proper motor speed. On the eight pole motor, 16.4 to 16.48ms should occur for five pulses, leading edge to leading edge. Adjustments can be made at R2.

3.5.1.2 Head Positioning Control

A stepper motor is used to turn a positioning screw on the head assembly to move the heads up and down. Signals TRO, TR1, TR2, and TR3 input to the Main Drive gate array processor contain the 4-bit code for the nine track selection. From the 4-bit code input, the gate array processor outputs to the stepper motor driver U18 with leads to the stepper motor windings through connector J4 to position the head assembly at the appropriate track. A reset signal to the gate array processor causes the head assembly to be positioned at track 0.

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3.5.1.3 BOT/EOT Sensing

BOT and EOT windows are detected by two photo transistors sensing light through holes punched in the tape. Tape position is indicated by the status of the Upper Tape Hole (UTH-) and Lower Tape Hole (LTH-) signals. The tape position codes are defined in table 3-11.

Table 3-11. Tape Position Codes

UTH- LTH- DEFINITION

True True BOT position

False True EOT position

- True False Warning Zone, between BOT and Load Point or between Early Warning and EOT.
- False False Recording Zone, between Load Point and Early Warning if a BOT or EOT position has occurred since the last cartridge insertion; otherwise, this code means the tape position is unknown

The gate array processor U12 issues UTH- and LTH- based on input from latches U13. When a tape hole is detected, the gate array processor receives input at pin 19. If the latches also pass a signal to pin 18 of the gate array processor, an upper hole is detected; if, however, the latches pass a signal to pin 17 of the gate array processor, a lower hole is detected. The gate array processor encodes the upper/lower tape hole input into the 2-bit tape position code.

3.5.1.4 Read/Write/Erase Signal Processing

Write data comes in at pins 9 and 10 of connector J8. Write Enable comes in at pin 29 of connector J8 to enable the gates to pass the data via transistors Q5 and Q4 to both write heads. Only the selected write head is enabled to write the data. When a write head is enabled, the erase bar is also activated to erase the tape immediately preceding the write head.

The write head (and also the read head) is selected by the state of TRO through transistor U9. Only one write head (or read head) is selected at any given time. When TRO is false, head 0 is selected; when TRO is true, head 1 is selected. During head positioning, however, head selection is disabled by STEPEN (stepper motor enabled) at transistor Q1. In addition, head selection is disabled by USF (unsafe) if the cartridge unsafe condition is detected.

Read data from the selected head is passed through read data amplifier U2, differentiated and filtered, passed through read data amplifier U1, and converted to logic levels by the comparator/limiter. Read-After-Write data passes through a threshold comparator to eliminate marginal recording areas from the tape that do not pass the nominal signal amplitude threshold. The time domain filter eliminates transitions of less than half a data transition period from the Read Data Level (RDL) signal. The Read Data Pulse (RDP) signal is generated at each transition of RDL and sent to the Formatter PCBA.

The Erase Bar on the head assembly is selected when TRO is false and EEN (erase enable) is asserted. This enables the erase driver for tape erasing.

3.5.2 Formatter PCBA

The block diagram shown in figure 3-6 illustrates the functions of formatting data to write to the tape or read from the tape and interfacing with the host.

3.5.2.1 Formatting Data

The Uncommitted Logic Array (ULA) U23 performs the data formatting function. The signals REFCLK and RDCLK are used in the phase lock loop to synchronize the read/write speed. The signals are compared to either pump up or pump down the voltage at the comparator U26. The data is also processed through the memory buffer U36 controlled by signals MEMIN, MEMOUT, and MEMWR.

Serial data read from the tape, RDP, comes from the Main Drive board to ULA pin 35. After processing, formatting, and buffering, the serial data, now HOUT, is sent from ULA pin 27 to serial-to-parallel converters U2 and U10 to be converted to parallel data. Parity for the data to the host is generated at U9, the parity generator/checker. The parallel data is gated on the bus to the host.

Parallel data sent from the host to be written on the tape comes in to parity generator/checker Ul3 and is converted to serial data by the parallel-to-serial converter Ul9. The serial data, HDIN, goes into the ULA at pin 45. The data is processed, formatted, and buffered before being sent to the Main Drive board as WDA+ and WDA-.

3.5.2.2 Host Interface

Host interface and data handshaking are performed by the Formatter board microprocessor U24. Commands from the host are received over the data bus. The commands and drive status are multiplexed into the microprocessor. Control signals are gated/latched to the drive and ULA U23 to process the read/write data and to handshake the data to/from the host.

Status data is sent from the microprocessor through the serial-to-parallel converters U2 and U10 and the parity generator/checker U9, then gated on the bus.

Command timing and sequence is described in paragraph 3.4.5.



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Figure 3-6. Formatter PCBA Block Diagram

SECTION IV

MAINTENANCE

4.1 GENERAL

This section contains information to aid the service representative in maintaining and troubleshooting the MCS. The section is divided as follows:

- o Preventive Maintenance
- o Cartridge Loading/Unloading
- o Troubleshooting
- o Alignment/Adjustment Procedures

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists primarily of cleaning the entire unit of dust and dirt and cleaning the magnetic read/write heads. The MCS assembly should be cleaned on a daily basis with a soft brush or a lint free cloth to prevent the accumulation of dust and dirt.

The read/write head assembly should be cleaned after approximately 20 hours of actual operation, in accordance with the following procedure:

1. Moisten a lint-free swab with Freon TF. Only use Freon TF to clean the head assembly.



Do not overmoisten the swab causing run off of the cleaning solution into the system. Improper operation or damage to the system could result from excessive solution run off into the internal assemblies. Never use a sharp instrument to clean the head(s); permanent damage can result from scratching.

- 2. Gently rub the swab on the head(s).
- 3. Allow the head assembly to dry thoroughly before operating the system.

4.3 CARTRIDGE LOADING AND UNLOADING

The cartridge tray loading mechanism is actuated by the front-mounted lever. The lever can be rotated through a full 90 degrees. With the lever in the horizontal position, the cartridge tray is released and ready for cartridge loading or unloading. With the lever in the vertical position, the inserted cartridge is secured in the operating position. Perform the following steps and refer to figure 4-1 to load and unload tape cartridges.

- 1. Insert the cartridge into the tray and push it into the drive (see figure 4-1, step #1). This aligns the outer edge of the cartridge with the front of the tray.
- Continue to push the cartridge and tray into the system (see figure 4-1, step #2). This automatically opens the cartridge protect door.
- When the cartridge is fully inserted, it is locked in place and correctly seated relative to the read/write head. Raise the front-mounted lever to the vertical position (see figure 4-1, step #3).
- 4. To unload the cartridge, move the lever to the horizontal position and remove the cartridge.



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Figure 4-1. Cartridge Loading

4.4 TROUBLE SHOOTING

Field level troubleshooting consists of isolating the fault to a major assembly and replacing that assembly. At this time, the PCBA's are considered part of the mechanical assembly and are not replaced independently. Consequently, if the actual mechanics or electronics are faulty, the entire mechanical assembly can be replaced according to the procedures in Section V.

4.5 ALIGNMENT AND ADJUSTMENT PROCEDURES

TBD

SECTION V

REMOVAL/REPLACEMENT

5.1 INTRODUCTION

This section contains removal and replacement procedures for the recommended field level major assembly replacement. If the spare parts or part numbers cannot be found on the drawings, tables, or part itself, contact the service branch manager and provide a description of the part and the MCS serial number.

5.2 PURPOSE

The purpose of this section is to aid service representatives and technicians in rapidly locating, identifying, and removing/replacing the major assemblies of the MCS.

NOTE

Refer to Engineering Change Notices for changes in parts lists and drawings not included in this revision of this manual. All Engineering Change Notices and relevant documentation should be kept with this manual.

5.3 REMOVAL AND REPLACEMENT

WARNING

To prevent injury from electrical shock, always disconnect the main power source before servicing the MCS.

The following paragraphs describe the removal and replacement (R/R) procedures for the various assemblies of the MCS. Two revision levels of the MCS may be encountered. The early revision MCS, prior to the nine hundred thousand series model number, is distinguished by two separate power supply assemblies screwed to the chassis and a line filter cable connected to the input line source, as illustrated in figure 5-1. The later revision of the MCS, nine hundred thousand series model number and subsequent, is distinguished by a single power supply board and a line filter directly connected to the input line source as illustrated in figure 5-2.



Early Configuration Major Assembly Removal and Replacement

The following paragraphs describe the R/R procedures for the major assemblies of the early configuration MCS, prior to nine hundred thousand series model numbers.

Mechanical Assembly Removal and Replacement

- 1. Remove system power and remove the top cover.
- 2. Disconnect the cable to the rear panel connector from the rear of the Formatter PCB.
- 3. Disconnect the cable to the power supply from the rear of the Main Drive PCB.
- 4. Remove the four (4) screws, two (2) on each side, securing the entire mechanical assembly and PCB's to the lower chassis.
- 5. Lift the entire assembly out of the enclosure.
- 6. To replace the assembly, perform these steps in reverse order.

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Line Filter Removal and Replacement

- 1. Remove system power and remove the top cover.
- 2. Disconnect the two (2) load wires to the power switch.
- 3. Disconnect the two (2) line wires to the line source and fuse.
- 4. Remove the two (2) screws securing the line filter to the chassis.
- 5. Remove the line filter.
- 6. To replace the line filter, perform these steps in reverse order.

Fan Removal and Replacement

- 1. Remove system power and remove the top cover.
- 2. Disconnect the cable from the fan to the power switch.
- 3. Remove the four (4) screws securing the fan and fan guard to the rear panel.
- 4. Remove the fan.
- 5. To replace the fan, perform these steps in the reverse order.

Power Supplies Removal and Replacement

- 1. Remove system power and remove the top cover.
- 2. Disconnect the cables to the power supply from the switch and the mechanical assembly.
- 3. Remove the four (4) screws securing the bottom chassis at each corner.
- 4. Remove the entire bottom chassis.
- 5. Remove the four (4) screws securing the appropriate power supply from the bottom of the chassis.
- 6. To replace the power supply, perform these steps in the reverse order.

Figure 5-1. Early Configuration Major Assembly Removal and Replacement



Later Configuration Major Assembly Removal and Replacement

The following paragraphs describe the R/R procedures for the major assemblies of the later configuration MCS, nine hundred thousand series model numbers and subsequent.

Mechanical Assembly Removal and Replacement

- 1. Remove system power and remove the top cover.
- 2. Disconnect the cable to the rear panel connector from the rear of the Formatter PCB.
- 3. Disconnect the cable to the power supply from the rear of the Main Drive PCB.
- 4. Remove the four (4) screws, two (2) on each side, securing the entire mechanical assembly and PCB's to the lower chassis.
- 5. Lift the entire assembly out of the enclosure.
- 6. To replace the assembly, perform these steps in reverse order.

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SECTION VI

ILLUSTRATED PARTS LIST

6.1 INTRODUCTION

This section provides parts list information for the MCS assemblies.

NOTE

Refer to Engineering Change Notices and related documents for changes to the parts list and for drawings not included in this revision of this manual. All changes should be kept with this manual.

6.2 ILLUSTRATED PARTS LIST INDEX

The illustrated parts list index provides the figure/ table number, title, and page number. Early configuration MCS assemblies are prior to the nine hundred thousand series model number; later configuration MCS assemblies are the nine hundred thousand series model number and subsequent.

FIGURE/TABLE	TITLE	PAGE
6-1	Early Configuration Assemblies	6-2
6-2	Later Configuration Assemblies	б-4
6-3	Main Drive PCBA	6-6
6-4	Formatter PCBA	6-10





Figure 6-1. MCS Assemblies, Early Configuration

Table 6-1. Early Configuration Parts List

FIGURE 6-1 INDEX NO.	DESCRIPTION	ICN DESIG- NATION	VENDOR PART NO.
1	Magnetic Tape Drive, 1/4 Inch Cartridge including the Mechanical Assembly,	MM540010	400412-001
	Main Drive PCBA		940084-003
	Formatter PCBA		960477-001
2	Housing, Top/Bottom		907406-001
3	Cover Assembly		907442-001
4	Front Bezel		907405-001
5	Chassis		907444-001
6	Power Supply, 12v	MM540030	400551-001
7	Power Supply, 5v	MM540020	400422-001
8 9	Line Filter EMI, 2A, 250vac Rocker Switch, 15A		181005-002
10	Recpt, ac Power Male GEE, 6A, 250v,		330002-001 315039-001
10	Pnl Mount		313039-001
12	Fan Guard, 3in		345017-001
13	Cable Assy, Ribbon, 50 Conn Edge to D-Sub		907174-014
14	Cable Assy, P/S MCS		907449-001
15	Jumper Assy, 18 AWG Sin gnd		906899-016
16	Jumper Assy, 18 AWG Sin		906899-017
17	Jumper Assy, 18 AWG 7in		906899-019
18	Cord Assy, Fan, 6in		902795-004
21	Screw, Hex HD, Self Locking, 6-32X.25		202013-001
22	Screw Hex Washer HD TF, 12-24X.50		204002-048
23	Screw Hex Washer HD THR Forming, 8-32		204002-019
24	Screw Hex Washer HD THR Forming, 10-32		204002-032
25	Screw, Hex HD, Self Locking, 10-32X.25		202013-006
26	Screw, Pan HD Phillips		202000-101
27	Nut KEP 4-40		214019-001
29	Wire, Ins, 300v, 80C, UL 1061, 18 AWG, White		784007-037
31	Plate Identification Assy		762130-001
33	Fuseholder Panel, Low Profole, 1/4 X 1-1/4		338010-001
34	Nut KEP 10-32		214019-008
35	Latch Spring		907484-001
36	Foot		907617-001
37	Lock Screw Assy, Female, 4-40		310006-001
38	Wire, Solid Unins AWG		786004-002
Bl	Fan, 110V	MM617010	345002
Bl	Fan, 220V (International Use)	MM540070	345002-001



Figure 6-2. MCS Assemblies, Later Configuration

Table 6-2. Later Configuration Parts List

FIGURE 6-2 INDEX NO.	DESCRIPTION	ICN DESIG- NATION	VENDOR PART NO.
2	Housing, Top/Bottom		907406-001
3	Cover Assembly		907442-001
4	Front Bezel		907405-001
5	Chassis		907654-001
б	Power Supply, 12/5V		400446-002
7	Streamer Cartridge Drive	MM54010	400412-001
	including the Mechanical Assembly,		
	Main Drive PCBA		940084-003
	Formatter PCBA		960477-001
8	Line Filter EMI		181021-001
9	Rocker Switch, 10A		330006-001
12	Fan Guard, 3in		345017-001
13	Cable Assy, Ribbon, 50 Conn Edge to		907174-014
	D-Sub		
14	Cable Assy, P/S MCS		907743-001
15	Jumper Assy, 18 AWG Sin gnd		906899-016
17	Jumper Assy, 18 AWG 7in		906899-019
21	Screw, Hex HD, Self Locking, 6-32X.25		202013-001
22	Screw HWH T/F 6-20X.25		204004-009
23	Screw HWH T/F 8-18X.25		204004-010
24	Screw HWH T/F 10-32		204002-030
25	Screw HWH Self Locking, 10-32X.25		202013-006
31	Plate Identification Assy		762130-001
34	Nut KEP 10-32		214019-008
35	Latch Spring		907484-001
36	Foot		907617-001
37	Lock Screw Assy, Female. 4-40		310006-001
39	Bracket, MTCS/Floppy/WDD		907655-001
40	Bracket, P/S Mounting		907657-001
Bl	Fan, 110V	MM617010	345002
Bl	Fan, 220V (International Use)	MM540070	345002-001



Figure 6-3. Main Drive PCBA 940084-001

Table 6-3. Main Drive PCBA 940084-001 Parts List

VENDOR PART NO.	DESCRIPTION	REFERENCE DESIGNATION
940084-101	PCB Main Board	REF
940084-300	Main Board Schematic	REF
102669-330	Cap, 33pF	Cl,17,23
101004-103	Cap, Cer, .01uF, 100v, 10%	C2,8,11,22,54
201244-104	Cap, Cer, .luF, 50v, 20%	C3-6,9,10,12,13,15, 18-21,27,28,31,33,
		34,39,41,46,50
102669-472	Cap, 4700pF	C7
101001-685	Cap, Tant, 6.8uF	C14
102871-225	Cap, Tant, 2.2uF, 20v	C16,42,43
102669-301	Cap, 300pF	C24,25
102669-750	Cap, 75pF	C26
101004-332	Cap, Cer, .0033uF, 100v, 10%	C29,47
102667-102	Cap, Cer, .OOluF, 100v, 10%	C30,58
102669-150	Cap, Cer, Axial Lead, 15pF, 5%,	a 20
201114 470	lOOwvdc, NPO TC Cap, Cer, .047uF, 50v, 10%	C32
201114-470 201113-220	Cap, Cer, 10470F, 50V, 10% Cap, Cer, 2200pF, 50V, 10%	C35,36 C37,59
102768-226	Cap, 22UF, 10v	C38
102669-331	Cap, 330pF	C40
201105-474	Cap, Cer, .47uF, 50v, 10%	C44
201160-220	Cap, Tant, 2.2uF, 35v, 10%	C45
102669-200	Cap, Cer, Axial Lead, 20pF, 5%,	
	lOOwvdc, NPO TC	C49
201160-681	Cap, Tant, 6.8uF, 35v, 10%	C51
102667-104	Cap, Cer, .luF, 100v, 10%	C52,53,61,62
950131-227	Cap, Tant, 220uF, 30v, 20%	C55
201213-056	Cap, Cer, 5600pF, 100v, 10%	C56 C57
201111-390 201148-220	Cap, Cer, 39pF, 50v, 10% Cap, PC, .22uF, 50v, 5%	C60
970161-001	Header, 4 Posn, RT Angle, PC Mount,	200
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Shrouded	J2
211000-107	Header, .100 Centers, Right Angle	J4
211000-113	Header, .100 Centers, Right Angle	J5
211000-109	Header, .100 Centers, Right Angle	J7
105008-013	Connector, 34 Pin	J8
120916-000	Connector, 7 Pin	J11,12
120916-001	Connector, 8 Pin	J13
101204-005	Connector, 34 Pin Socket	P9
106500-1.14	Crystal, 3.579 MHz	Y1,2
107201-001 125017-012	Diode, High Conductance, High Speed Voltage Regulator, 78L12	CR1-10
203013-210	IC Voltage Regulator, 78112	VR1 VR2
203013 210	TO VOICAGE REGULACOL	V 1(2)

Table 6-3. Main Drive PCBA 940084-001 Parts List (continued)

VENDOR PART NO.	DESCRIPTION	REFERENCE DESIGNATION
FART NO.	DESCRIPTION	DESIGNATION
122502-006	Inductor, 240uH	LI,3,4
122502-003	Inductor, 56uH	L2,5
122502-001	Inductor, Molded Axial Lead	L6
122500-001	Inductor, Shielded SWD-220 G.C.	L7
151030-001	Transistor, 2N3904	Q1,4,5
151033-001	Transistor, MM3007	Q2,3
204013-999	Transistor, NPN Silicon	Q6,7
101032-001	IC, 592	Ul,2
123239-001	IC, 319	U3
123029-001	IC, Quad 2 Input Nand Gate	U4
100331-001	IC, 7406	U5
123038-001	IC, 75LS86	U6
123036-001	IC, Dual D Type Flip-Flop	U7,13
123031-001	IC, Ifex Inverter	U8,14,16
151032-001	IC, Q2T2905	U9
100234-001	IC, 9602	U10
203007-393	IC, Comparator	U11,U26
960925-001	IC, Gate Array Processor	U12
101139-001	IC, 75451	U15
123123-001	IC, 74LS09	U17
970164-001	IC, Drivers, Power, Quad, Nand Gate	U18
970229-001	IC, Timer/Counter, Programmable	U19
123035-001	IC, Quad, 2-Input Or Gate	U20
123155-001	IC, 74221	U21
970150-001	IC, Op-Amp/Voltage Comp	U22
960453-001	IC, Software Assy, Motor Control	U23
142016-005	IC, Res Network, 2.2K SIP	U24
125043-001	IC, 556	U25
203007-358	IC, Op-Amp/Buffer, Dual IC, Driver, Motor, Half-Bridge	U27 U28,29,30
970165-001 123041-001	IC, 74LS193	U28,29,30 U31
138002-103	Potentiometer, 10K Ohm	Rl
200209-202	Potentiometer, Cer, 2K Ohm	R1 R2
100155-385	Res, 10K Ohm, 1/4W, 1%	R3,27,31,38,87,88
101156-203	Res, 20K Ohm, 1/4W, 5%	R4,37
100155-415	Res, 20.5K Ohm, 1/4W, 1%	R5,11
101156-102	Res, Carbon Film, IK Ohms, 1/4W, 5%	R6,9,16,45,64,75,7
101100 101		90,94
101156-100	Res, 10 Ohm, 1/4W, 5%	R7,62,63
100155-347	Res, 4.02K Ohm, 1/4W, 1%	R8.10
101156-511	Res, 510 Ohm, 1/4W, 5%	R12,13,42-44,67,828,
100155-351	Res, 4.42K Ohm, 1/4W, 1%	R14,32,33
101156-472	Res, Carbon Film, 4.7K Ohm, 1/4W, 5%	R17,23,35,65,81
101156-103	Res, 10K Ohm, 1/4W, 5%	R15,93
101156-471	Res, 470 Ohm, 1/4W, 5%	R18,19
101156-513	Res, 51K Ohm, 1/4W, 5%	R20
101156-473	Res, Carbon Film, 47K Ohm, 1/4W, 5%	R21,95

Table 6-3. Main Drive PCBA 940084-001 Parts List (continued)

VENDOR		REFERENCE
PART NO.	DESCRIPTION	DESIGNATION
101156-222	Res, 2.2K Ohm, 1/4W, 5%	R22,49
101156-392	Res, 3.9K Ohm, 1/4W, 5%	R24
100155-463	Res, 64.9K Ohm, 1/4W, 1%	R25
200076-330	Res, FC, 330 Megohm, 1/4W, 5%	R26
138002-104	Potentiometer, 100K Ohm, 1/2W	R28
101156-333	Res, 33k Ohm, 1/4W, 5%	R29,30
101156-303	Res, 30K Ohm, 1/4W, 5%	R34
100155-437	Res, 34.8K Ohm, 1/4W, 1%	R36
101156-133	Res, 13.3K Ohm, 1/4W, 1%	R39
100155-289	Res, Metal Film, IK Ohm, 1/4W, 1%	R40,41,85,86
101156-822	Res, 8.2K Ohm, 1/4W, 5%	R46
101156-390	Res, 39 Ohm, 1/4W, 5%	R47
101156-131	Res, 130 Ohm, 1/4W, 5%	R48
200771-510	Res, Fxd, Crb Flm, 51 Ohm, 1/4W, 5%	R50
101156-121	Res, 120 Ohm, 1/4W, 5%	R51,52
101156-681	Res, 680 Ohm, 1/4W, 5%	R53,54
100155-254	Res, 432 Ohm, 1/4W, 1%	R55
101156-153	Res, 15K Ohm, 1/4W, 5%	R56,57
200772-100	Res, Fixed, Carbon Film, 100 Ohms,	
	1/4W, 5%	R58
100155-346	Res, 3.92k Ohm, 1/4W, 1%	R59,60
200120-500	Res, WW, 5 Ohm, 3.75W, 5%	R61
101156-473	Res, 47K Ohm, 1/4W, 5%	R66
101156-682	Res, 6.8K Ohm, 1/4W, 5%	R70,79,80
101156-122	Res, 1.2K Ohm, 1/4W, 5%	R71,76
100155-164	Res, 49.9 Ohm, 1/4W, 1%	R72
100155-232	Res, 255 Ohm, 1/4W, 1%	R73
200075-470	Res, FC, 470K Ohm, 1/4W, 5%	R74
200772-220		R77
970314-001	Res, 62 Ohm, 1W, 5%	R83
970299-001	Res, WW, .10 Ohm, 1W, 10%	R84
101156-302	Res, 3K Ohm	R89
101156-152	Res, 1.5K Ohm, 1/4W, 5%	R91,92
146014-040	IC Socket, 40 Posn	XU12
146014-016	IC Socket, 16 Posn	XU18,23
100360-001	Pin, Wire Wrap, .025sq, .3171g	TP1-10,E1-3,E6-13
210875-501	Insulator, Thermally Conductive	U28,29,30


Figure 6-4. Formatter PCBA 960477-001

Table 6-4. Formatter PCBA 960477-001 Parts List

VENDOR PART NO.	DESCRIPTION	REFERENCE DESIGNATION
960477-101	PCB Formatter	REF
960477-300	Formatter Schematic	REF
201244-104	Cap, Cer, .luF, 50v, 20%	Cl-4,9,10,20-25,27, 28
101002-255	Cap, Tant, 2.2uF, 20v, 10%	C5
102669-561	Cap, Cer, Axial Lead, 560pF, 100wvdc, 5%, NPO TC	, C6
100165-103	Cap, Mylar Film, .0luF, 100v, 10%	C8
101001-226	Cap, Tant, 22uF, 6v, 10%	Cll
102669-472	Cap, Cer, 4700pF, 10%	C12
101001-225	Cap, Tant, 2.2uF, 6v, 10%	C15
100243-391	Cap, Dipped Mica, 390pF	C16-18
102669-150	Cap, Cer, Axial Lead, 15pF, 100wvdc, %5, NPO TC	C19
102669-200	Cap, Cer, Axial Lead, 20pF, 100wvdc,	
		C26,29
122502-001	Inductor, Molded Axial Lead	LI
202006-100	Diode, Light Emitting, Red	DS1
107201-001	Diode, High Conductance, High Speed	CR1,2
950101-034	Connector, Rt Angle, 100 Centers	J9
125038-003	Hybrid Clock 1C	Yl
106500-116	Crystal, Quartz, Wire Leads	Y2
100336-001	IC, Quad 2 Input Nand Buffer	U1,3,7,11,32
123233-101	IC, 4 Bit Parallel Access Sft Reg	U2,10
123001-001	IC, Hex Schmitt Trigger Inverter	U5,6,12
101022-001	IC, Voltage Comparator	U8
950103-001	IC, 9 Bit Odd/Even Par Gen/Ckr	U9,13
123040-001	IC, Quad 2 Line to 1 Line Mux	U14,20
123036-001	IC, Dual D Type Flip-Flop	U15,22,25,27
123096-001	IC, Hex D Flip-Flop	U16,17,34
123237-001	IC, Octal Trans Latch	U18
123232-101	IC, 8 Bit Para In/Serial Out Sft Reg	U19
123100-001	IC, Decoder/Demux, 3 Line to 8 Line	U21
960430-001	IC, Schem Cartridge Tape Data Fmtr	U23
940189-003	IC, Single Dip, 8 Bit, 8751	U24
100345-001	IC, Detector, Phase Frequency	U26
123125-001	IC, Dual 4 Input And Gate	U28
123031-001	IC, Hex Inverter	U29
123043-001	IC, Dual Monostable Multivibrator	U30.31
123029-001	IC, Quad 2 Input Nand Gate	U33
207027-001	IC, Assy, 256 x 4 Host Sequencer	U35
950104-001	IC, Static RAM, 16K x 1 Bit, 6167	U36
123203-001	IC, Dual 4 Stage Binary Counter	U37
123235-001	IC, 12 Stg Ripple Carry Bin Ctr/Dvdr	
123035-001	IC, Quad 2 Input Or Gate	U39
123032-001	IC, Quad 2 Input And Gate	U40

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Table 6-4. Formatter PCBA 960477-001 Parts List (continued)

VENDOR		REFERENCE
PART NO.	DESCRIPTION	DESIGNATION
101156-331	Res, Crb Flm, 330 Ohm, 1/4W, 5%	Rl
101156-221	Res, Crb Flm, 220 Ohm, 1/4W, 5%	R2,10
101156-472	Res, Crb Flm, 4.7K Ohm, 1/4W, 5%	R3,20,24
101156-105	Res, Crb Flm, 1 Megohm, 1/4W, 5%	R4
101156-473	Res, Crb Flm, 47K Ohm, 1/4W, 5%	R5
101156-244	Res, Crb Flm, 240K Ohm, 1/4W, 5%	R6
101156-102	Res, Crb Flm, 1K Ohm, 1/4W, 5%	R7,8,23,25
101156-271	Res, Crb Flm, 270 Ohm, 1/4W, 5%	R9,21
100155-239	Res, Mtl Flm, 301 Ohm, 1/4W, 1%	R11.13
100155-289	Res, Mtl Flm, 1K Ohm, 1/4W, 1%	R12
100155-327	Res, Mtl Flm, 2.49K Ohm, 1/4W, 1%	R14-16
100155-339	Res, Mtl Flm, 3.32K Ohm, 1/4W, 1%	R17-19
101156-391	Res, Crb Flm, 390 Ohm, 1/4W, 5%	R22
205254-500	Res, Network, 51 Pin, 4.7K Ohm	UR1
142021-001	Res, Network, 10 Pin,	UR2
142032-001	Res, Network, 16 Pin, 5%	U4
146014-016	IC Socket, 16 Posn	XU4
950110-001	IC Socket, 48 Pin	XU23
146014-040	IC Socket, 40 Posn	XU24
205025-620	IC Socket, 20 Contacts	XU36
100360-001	Pin Wire Wrap, .025sq, .3171g	W5-9,TP1-3

SECTION VII

REFERENCE DATA

TITLE	FIGURE NUMBER	PAGE
Main Drive PCB Schematic	7-1	7-3/4
Formatter PCB Schematic	7-2	7-9/10





Figure 7-1. Main Drive Schematic (Cipher 940084-300 Rev. A) (Sht 1 of 3)

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Figure 7-1. Main Drive Schematic (Cipher 940084-300 Rev. A) (Sht 2 of 3)



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Figure 7-1. Main Drive Schematic (Cipher 940084-300 Rev.A) (Sht 3 of 3)

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R23 ENABLE DAMERS 7438 U32 6 MV5053 DISABLE DRIVERS U33 DSI A 21 5 U32 1500 5 **J9** 74 30 (HADA 8-2 (54-2) 7 KEY K 3 TACH UNDR 1 2 UNDR 1 2 UNDR 2 1 FEARST (SH-2) CHADR O - 15-18,21 +5V U21 CHADR I C1-4,9,10,14, 20-25,27,28 + 411 TP-3 CHADR 2 LSI38 ۱. 12 (8,11,12,14,22, 24,26,28,30,32)GROUND 11 10 9 5. 20 TR2 20 TR2 23 TR1 29 TR0 BUS 7 CHSEL (SHI42) 52 610 **UI7** 2056 U15 1574 UISP 4 12 +SV SURI 5218 L5174 17 DSCRP -11 1574 (5H-2) 2154 1 10 8JS 3 13 12 12 13? K34 NUS BUS 2 11 9 4 (HBN 3 7 8 9 BUS 7 BUS 7 WEN (SH-2) THBUS & 6 BUSG BUSS 4 7 016 **u18** CHEWS 5 4 5 EUSS ĉus 5 6 CHEUS 4 3 15373 LSI74 2 BUS4 BUS 4 11 10 K27 REV K31 GO CHEWS 3 19 CHEWS 2 17 19 BUS 3 BUS 3 13 16 BUS2 CHEUS 1 14 CHENS & 13 12 EUS 0 KI RST-BUS 9-7 (SH-2) 50-7 ₹ AST (SH-162) <4 UTH-W6 PARITY ERROR (SH-2) W5 12 14 HIN3 KS USF-UI4 5 3 KG CIN-4 L\$157 2 HINZ KZLTH-₩9 10 9 4 11 HINS SELI 7 6 5 HINA ±15 کوبך 4 W7 CF 5 14 HINT 12 U20 ino. WB W9 UNIT OFF CFF 1 ON CFF 2 OFF CN 3 CI: ON 4 9 11 HING L\$157 7 JUMPERS WAL W9: UNIT SELECT SHINI ¥8.0 7 4 2 HIND **1**³ JUMPER WG : PARITY CHECK OPTION. LURIS ş +5∀ - HIN 0-7 (SH-2)

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Figure 7-2. Formatter Schematic (Cipher 960477-300 Rev. A) (Sht 1 of 2)





Figure 7-1. Formatter Schematic (Cipher 960477-300 Rev. A) (Sht 2 of 2)