Basic Four®
System S/10 (Machine Type 4399)
Office Display Terminal (Machine Type 4398)
Service Manual

April 1983

BFISD 8072PA

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PREFACE

This manual contains the necessary information to install, repair and maintain the System S/10 and Office Display Terminal. The information in this manual is directed primarily toward the System S/10. For purpose of maintenance, the Office Display Terminal is the same unit without the Disk Drive assembly and Floppy Controller that supports the Disk Drive interface. The instructions and information are presented to aid maintenance personnel in the installation, operation and care of this system. All controls are described and operational considerations are presented in sufficient detail to enable field service personnel to operate and maintain the equipment.

The major topics described in this manual are:

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications, as temporarily permitted by regulation. It has not been tested for compliance with the limits for Class A Computing Devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the User at his own expense will be required to take whatever measures may be required to correct the interference.

SYSTEM S/10

OFFICE DISPLAY TERMINAL

8072-01

Figure 1-1. System S/10 and Office Display Terminal

SECTION I

INTRODUCTION

1.1 PURPOSE

This manual is a reference guide for the service technician. The information in this manual enables a service technician to maintain the S/10 System (S/10) or Office Display Terminal (ODT). See figure 1-1. It includes information and procedures needed to troubleshoot and maintain the S/10 or Office Display Terminal to the replaceable assembly level. All references to the System S/10 are applicable to the Office Display Terminal except where noted.

1.2 RELATED DOCUMENTS

This manual provides only the information necessary for a technician to service the S/10 or Office Display Terminal. Other documents that may be helpful to the service technician include the following:

- System S/10 Users Guide (BFBPC 4410)
- Office Display Terminal Users Guide (BFBPC 4400)

1.3 SAFETY PRECAUTIONS

As with any electronic equipment, precautions consistent with all standard industrial safety practices must be taken while servicing the S/10-ODT. The cabinet contains potentially dangerous voltages. Any servicing that requires removing cabinet covers must be performed by qualified service personnel. Before inspecting or servicing the S/10-ODT, disconnect power.

Notices are included throughout this manual to alert you to problem areas or situations that could cause personal injury, loss of data, or hardware damage.

A WARNING precedes the text of procedures; if not strictly followed could result in serious injury to the service technician.

A CAUTION precedes the text of procedures; if not strictly followed could result in the loss of data or damage to or the destruction of equipment.

A NOTE highlights essential procedures, conditions, or clarifying facts. NOTEs also provide information that helps the reader understand a concept or the completion of a procedure.

The following are general safety precautions that are not related to any specific procedure and therefore do not appear elsewhere in this manual. Personnel must heed these warnings during routine service and repair.

WARNING

Keep Away From Live Circuits.

Always observe safety precautions. Observe all the CAUTIONS and WARNINGS in this manual when working inside the equipment cabinet. Under certain conditions, dangerous potentials can exist when the power is off because of charges retained by capacitors or the cathode ray tube (CRT). To avoid injury, always remove power and discharge a circuit to ground before touching it.

The following WARNING applies to any service inside the equipment cabinet. It appears elsewhere in the text of this manual and is introduced here for emphasis:

WARNING

Hazardous voltages are exposed in the cabinet. Be extremely careful when servicing either the power supply or any area where power terminals are exposed.

1.4 S/10 OVERVIEW

The S/10 is a software based video display information station that combines state-of-the-art hardware and software technology with a design oriented to the user and his environment. The unit functions both as a stand alone processor and as a remote terminal for communication with a host computer. The Office Display Terminal (ODT) functions only as a remote terminal for communications with a host computer.

The keyboard has been designed to accommodate touch typing techniques using the layout and touch of a sculptured keyboard similar to that of popular office typewriters. The eye-easing high resolution display maximizes user productivity. From the keyboard the operator can control nearly all of the user convenience features including margin bell, audible keyclick, scroll rate, auto repeat, line width and screen intensity. Combined with a detachable, fold-up keyboard and an aesthetic, low profile design, the S/10 is a unique and flexible product for the modern office.

As a stand alone computer system, the S/10 provides ample local storage and ease of operation. The unit operates using the (BBM/CPM) operating system, for which a large body of application software exists. In this mode the unit can be used for word processing, accounting, inventory, data entry, and a variety of other applications.

The S/10 can also operate as a remote terminal. A variety of terminal personalities are available or planned which facilitate communication with different host computer systems. These personalities are stored on disk and loaded into the unit as needed.

The S/10 allows configuration of the operating characteristics of the system via software control, including definition and downloading of character fonts. User defined character fonts can be configured to provide unique characters for word processing and multi-lingual applications as well as line drawing and special graphic symbols. A dynamic memory manager efficiently allocates display memory on an as needed basis, providing the user with the optimum number of pages of data storage. The S/10 features and adaptability make it the ideal solution for a wide variety of applications and developmental needs.

1.5 PHYSICAL DESCRIPTION

1.5.1 Office Display Terminal (ODT)

The ODT Terminal is designed to work interactively with a host computer using either ANSI standards or a specific personality or protocol for the communications link. The personality is stored in the terminal in a Read-Only-Memory to enable it to interface with the host computer.

The ODT includes the following components:

a. Keyboard - The terminal has a unique hinged detachable keyboard that folds up out of the way when not in use, and also protects the face of the CRT. The keyboard, which is laid out like an office typewriter, is designed for the touch typist. It has sculptured keys, a 10-key numeric pad, and eight function keys (PF1 - PF8) which can be programmed by the user.

b. Display Monitor - The terminal features a P-4 white phosphor or a P-31 green phosphor screen as standard. (A green phosphor eases eye strain during extended periods of viewing.) The screen measures 12 inches diagonally.

c. Video Monitor Board - This circuit board performs the final stage of the video processing for the CRT screen display. It is mounted on the mother board.

d. Mother Board - This board is placed horizontally on the bottom of the console. All circuit boards are plugged into this board, which eliminates the need for interconnect cables and greatly improves the reliability of the unit. The speaker is mounted on this board.

e. Power Supply - This unit plugs into the Mother board, and supplies +5 volts, and ±12 volts. There is one adjustment on this unit to set the +5 volt level. The Power Supply for the System S/10 is of different current rating.

f. Advanced Processor (AVP) Board - This board plugs into the Mother board and carries all of the electronics required for the terminal. This includes the Z80 microprocessor, memory, NVR (Non-Volatile RAM), video processors, timing circuits, and circuits to support the serial data ports. The AVP Board for the System S/10 has slight differences in IC component configuration.

1.5.2 System S/10

The System S/10 is a stand-alone computer, which provides two diskette drives with controller, and the necessary Z80 micropocessor and memories to enable text and data processing. The computer is CP/M or BB/M based, giving a wealth of software which can be used with the computer.

The System S/10 is built with modular construction, using the same terminal assemblies listed for the ODT, but adding the following assemblies to turn the terminal into a computerized system. The exceptions are the power supply, which is bigger to provide more power for the additional circuits, disk drives for program storage, different configuration of the Advanced Processor (AVP) Board, and a controller board for control and data handling of the disk drives.

a. Advanced Floppy Controller Board (AFC) - This board plugs into the Mother board adjacent to the Advanced Processor board. It contains a second Z80 microprocessor, with 64K Random-Access Memory (RAM) and a Read-Only Memory (ROM) which "boots" the computer part of the system and loads the operating system. It also has the controller and other circuits for control and data handling for the diskette drive.

b. Diskette Drives - These are MPI drives which are double-sided double density 96tpi. These drives are shrouded in an aluminum box for screening.

c. Advanced Video Processor Board (AVP) - The AVP Board for the S/10 is the same as in the ODT except in the S/10 it contains 64K RAM, while the ODT AVP Board has 16K of RAM.

1.5.3 Main Console

The assemblies are contained in a high-impact plastic cabinet. The same cabinet is used for both the ODT terminal and the System S/10; only the blank panel to the right of the display is replaced with one with slots when diskette drives are installed. (See figure 1-2.)

The Power Supply, the Advanced Processor board, and the Advanced Floppy Controller board are held in place by the clamshell lid when it is lowered and locked in place.

1.5.4 Keyboard Assembly

The keyboard assembly is an integral unit consisting of a regulator, and the keypad assembly which are mounted on a printed circuit board. The keyboard is connected to the main console with a standard 4-wire coiled telephone cable allowing the keyboard to be detached and operated away from the display in a position to suit the operator. (See figure 1-3.)

Data to the keyboard is transmitted to the main unit via a USART (universal synchronous-asynchronous receiver-transmitter) located on the AVP board. The same keyboard is used for both the ODT and System S/10.

1.6 OPERATIONAL DESCRIPTION

The S/10 is an easy to operate data processing workstation and remote terminal. The unit can be considered as a typewriter that uses a video screen instead of paper and is a vehicle through which the operator is able to manipulate information and communicate with a computer. When a paper copy of information is needed, the information is sent to a separate printer unit.

The unit has several components which work together to form a self-contained system. The heart of the system is the central processing unit or CPU, which monitors and controls the other parts, and the main memory, which stores both instructions (programs) and information (data) used by the CPU. The main memory's content changes constantly when the unit is in use, and the content is lost when the unit is powered down; when the unit is turned on, it takes several seconds to load the instructions the unit needs to operate into main memory.

The keyboard, screen and disk drives are all devices which exchange programs and data with the CPU and main memory. The keyboard is the primary means for the user to communicate with the system. The screen displays the result of the user's commands and the actions of the other components. The disk drives provide a permanent form of storage, as opposed to the temporary storage in the main memory. The drives write data from the main memory onto the magnetic surface of the floppy disks to make a permanent record. The drives also read data written on the disks into the main memory for use by the other components. In this way the user can store and manipulate large quantities of data.

When the S/10 is used by itself, the screen and keyboard provide the functions of a terminal. A terminal is a device which receives and displays data from a computer and also prepares and sends data back to the computer. The S/10 CPU and main memory act as an independent computer. A second section of memory, display memory, keeps a record of these transactions between the terminal part of the S/10 and the computer part of the S/10. This memory is completely separate from the S/10 main memory. Like the main memory, its contents change constantly and are lost when the unit is turned off.

A second way to use the S/10 terminal is to communicate with a host computer. When used in this way, the host computer provides CPU, main memory and permanent storage. The S/10 provides the screen, keyboard, and display memory.

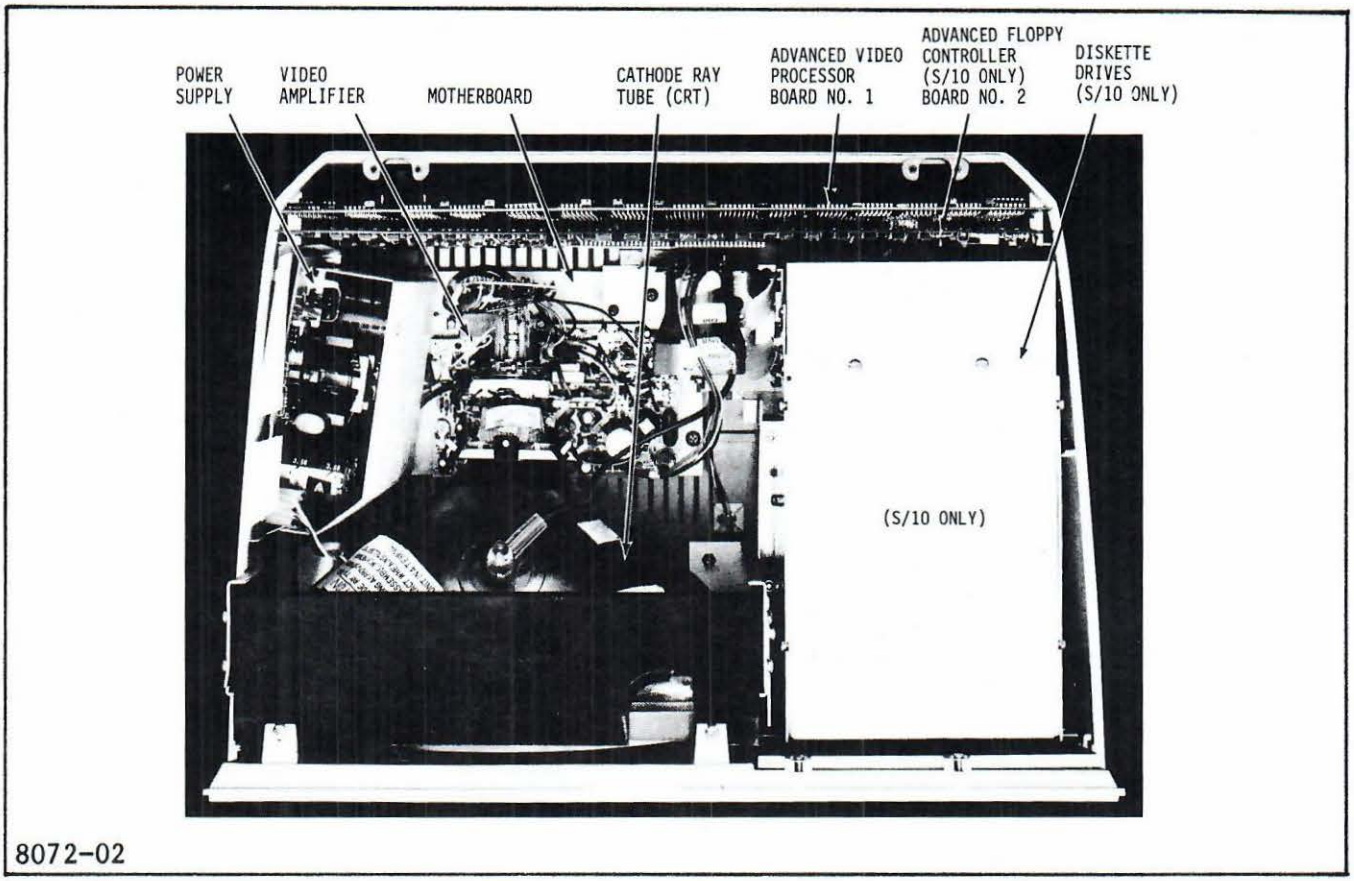

Figure 1-2. S/10-ODT Internal Components

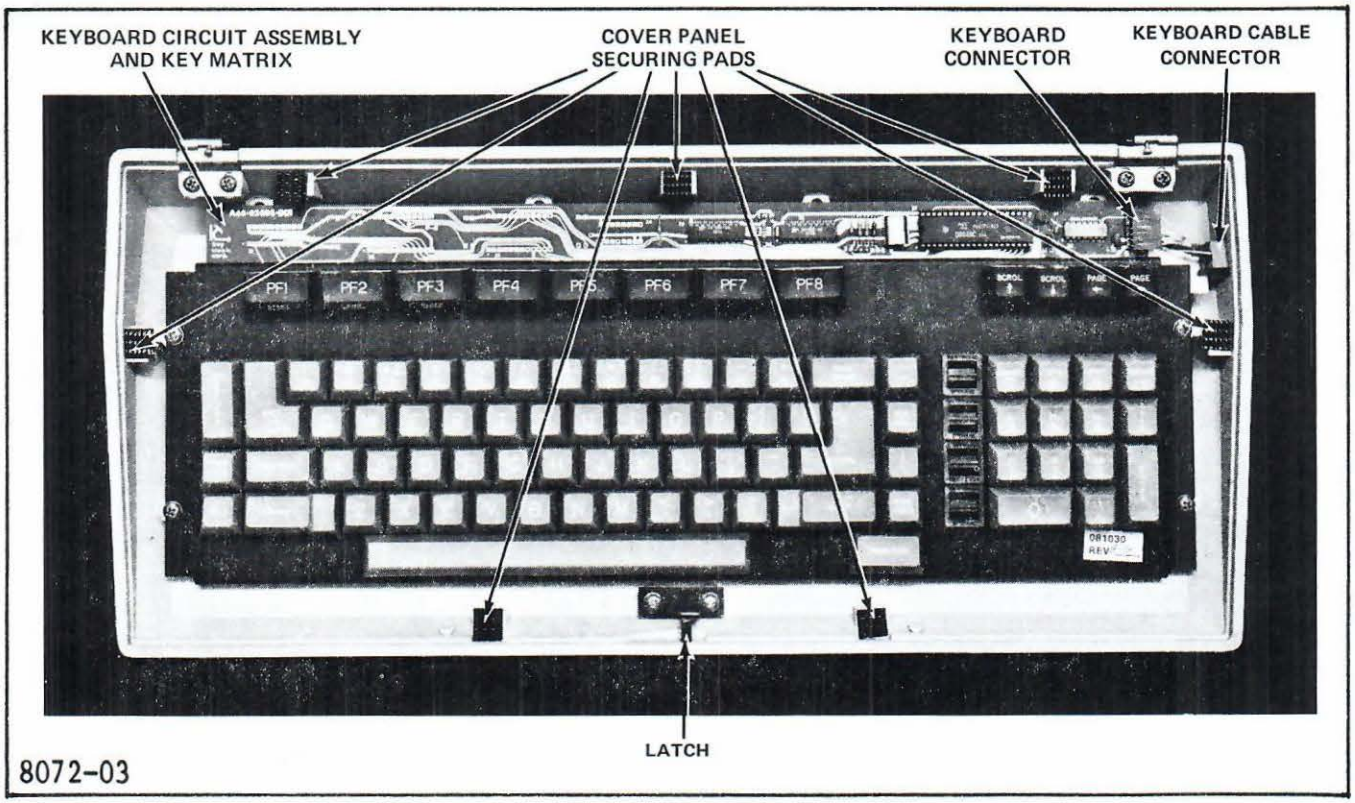

Figure 1-3. Keyboard Assembly

The display memory keeps a record of the data sent to the host computer and the host computer's responses. The S/10 CPU and main memory are not used when the S/10 communicates with a host computer.

The user does not have to keep track of the different types of S/10 memory when it is used for these different purposes; the unit keeps track of them automatically.

Figure 1-4 is a conceptual diagram of the S/10. It illustrates the flow of data among the various parts of the S/10, the printer, and the host computer.

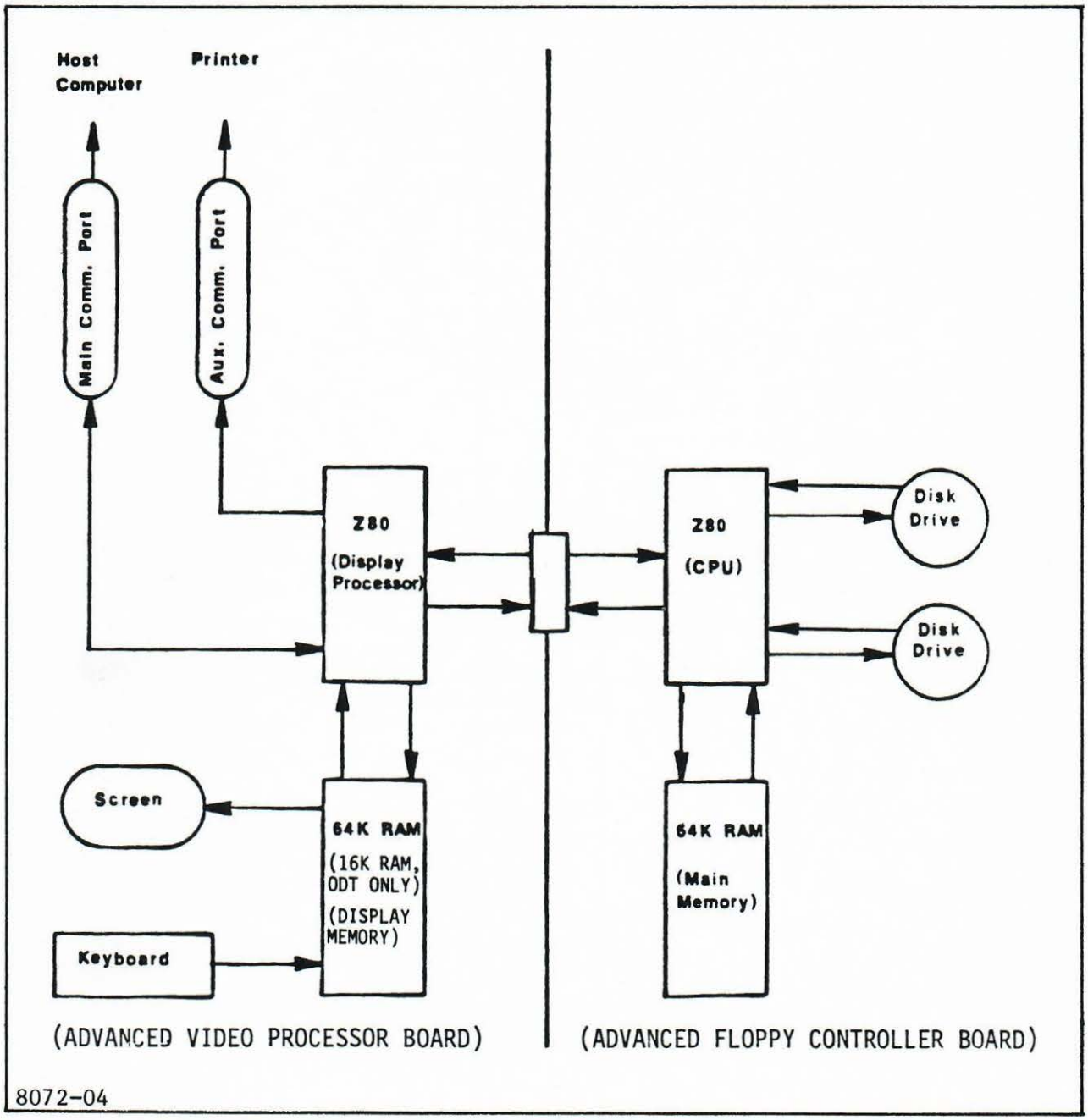

Figure 1-4. S/10 Conceptual Diagram

1.7 SPECIFICATIONS

The unit functions as a stand-alone processing station or as an Office Display Terminal to interact with a host computer. BBM/CPM is the operating system software. The Office Display Terminal (ODT) operates with 7270 emulation or or other specific protocols with a host computer. The specifications for the System S/10 and the Office Display Terminal are given in table 1-1.

Table 1-1. Specifications

PARAMETERS	CHARACTERISTICS
PHYSICAL	
Width	20.0 inches (500 mm)
Depth (Keyboard down)	22.0 inches (589 mm)
Height	11.75 inches (292 mm)
Weight ODT	30 lbs (13.6 Kg)
S/10	40 lbs (18.2 Kg)
ELECTRICAL	
Power	100/120VAC @ 2.5A 220/240VAC @ 1.5A
Frequency	50/60 HZ
OPERATING ENVIRONMENT	
Temperature	32°F to 95°F (0°F to 35°C)
GENERAL	
Display	12-inch diagonal screen with P-4 white or P31 green phosphor. 25 lines of 80 characters with line 25 (bottom) for status data, or 28 lines of 132 characters and line 29 for status data.
Keyboard	Standard typewriter style ANSI series keyboard, with alphanumeric keys, control keys, keypad, and eight programmable keys (96 keys total)
Processors	ODT - One Z80 microprocessor mounted on the AVP board, which controls the keyboard, display and I/O ports. Operates at 4.6MHz.

Table 1-1. Specifications (continued)

PARAMETERS	CHARACTERISTICS
Processors (cond't)	System S/10 - Two Z80 microprocessors, one mounted on the AVP board with the same functions as the ODT. A second Z80 microprocessor is mounted on the Controller board, operating at 4.6MHz, runs the Disk Controller and loads and runs the programs.
Floppy Disk Drive (S/10 Only)	Two 5 1/4-inch floppy diskettes: -622K bytes per diskette, double-sided, 96 TPI
5.25-Inch Hard Disk (S/10 Option)	10.49 Megabytes (2 disks) or 20.97 Megabytes (4 disks)
Memory	ODT - Z80 with 64K bytes of RAM for temporary storage. 4K bytes PROM to load the personality, and 16K PROM for protocol. S/10 - Z80 with 64K bytes of RAM mounted on AVP board for Display, Keyboard, and I/O Port functions. 4K bytes mounted on Controller board for diskette programs. Personalities are loaded from Program disk. 64K bytes of RAM on AFC board.

SECTION II

INSTALLATION

2.1 INTRODUCTION

The S/10-ODT are desk-top units designed to work in a normal office environment, and hence there are few constraints on the selection of a suitable location. Extremely high temperatures and levels of humidity should be avoided, and power MUST be free of surges and interruptions.

The unit is fully tested at the factory and is in full working order when shipped. It is ready to be plugged into a power receptacle and operated.

2.2 UNPACKING AND INSPECTING THE S/10-ODT

The unit is shipped in one carton, which includes the main unit, the keyboard, cables for power and the keyboard, and a Users Manual which contains the SYSTEM diskette (S/10 Only). Examine the carton upon arrival for signs of damage and mishandling. Any damage sustained during shipment is the responsibility of the shipper.

Place the carton in an upright position and open it. First lift out the keyboard, then lift out the unit and place it on a flat surface. Check for any signs of damage.

2.3 PREINSTALLATION CHECKS

Before connecting the unit to site power, the following checks should be made to prevent electrical damage to the equipment.

2.3.1 AC Power Requirements

Verify the following AC line requirements:

1. The AC line is not shared by devices that cause large transients (example: air conditioners, heaters, welding equipment or other equipment with large motors).

2. The AC line is not subject to voltage variations greater than 10%, or frequency variations greater than 0.2%.

3. The AC power outlets are the proper voltage (110 VAC, 60 Hertz) or 220 VAC, 50 Hertz, as applicable) and near enough to the equipment so that power extension cables are not necessary.

2.3.2 Ground Checks

1. Verify that power is not applied and the AC line cord is not connected before making the following checks.

CAUTION

Only three-wire connectors and three-pronged plugs with the third wire connected to earth ground are acceptable electrical connectors. NO two-wire connectors or plugs, with or without connection to a conduit ground, are to be used. Unstable equipment operation may result.

2. Check that the AC line includes a third-wire earth ground that meets or exceeds the requirements of the National Electrical Code. This can be checked as follows:

   a. Locate the circuit breaker that is to supply power to the cabinet. With a digital voltmeter set to measure 20 volts AC, and the circuit breaker turned ON, measure the drop between the green and white wires at the power source (wall outlets). The measured voltage must be less than 1.8 volts AC.

   b. Set the source circuit breaker to OFF. Measure the resistance between the green and white wires at the wall outlet. The resistance must be less than the value shown below for the circuit breaker rating.

Circuit Breaker Rating	Resistance
15 Amperes	0.30 Ohms
20 Amperes	0.25 Ohms
30 Amperes	0.15 Ohms

   c. If either measurement in steps a or b above is not less than or equal to the value given, request the customer to provide a power source that meets the given requirements.

2.4 POWER REQUIREMENTS

The power requirements of the S/10-ODT are uncomplicated. Ordinary wall outlets will supply the S/10-ODT with the proper power. Specific requirements are:

Voltage	115VAC at 2.5 Amps
Line Frequency	60Hz

or

Voltage	230VAC at 1.2 Amps
Line Frequency	50Hz

The unit as shipped matches the power supply available to the user. If the unit does not match the supply, a simple conversion can be performed. The conversion of the power supply must be done at the factory or by factory authorized service technicians.

2.5 INSTALLING THE S/10-ODT

The S/10-ODT is very easy to install. The shipping carton contains everything you need to set up a self-contained workstation. This selection gives all the preliminary directions you will need to follow.

The shipping carton contains the following:

a. The main unit, consisting of the CRT screen and disk drives.

b. The keyboard, wrapped separately in bubble wrap.

c. The power and keyboard cables, in a separate plastic bag.

d. Binder containing this manual and floppy disket (with S/10 only)

To prepare your unit for use, follow these steps:

1. Unpack all parts. Save the packing and shipping carton in case you need to move the unit at a later date.

2. Remove the main unit from the shipping carton and place it on any convenient surface, such as a desk, table or stand. Do not use a plush or spongy surface, such as a typewriter pad, which might restrict the airflow through the bottom vents. There also needs to be space for airflow through the vents on the sides, top and back.

3. Remove the keyboard from the bubble wrapping and place it in front of the main unit.

4. Remove the coiled keyboard cord from the shipping bag and plug one end into the receptacle on the right side of the keyboard. Plug the other end into the keyboard cord receptacle located on the lower left-rear of the unit, as seen from behind. (See figure 2-1).

CAUTION

Avoid plugging the unit into a wall receptacle with the power switch in the ON position. This can cause damage to the unit.

5. Remove the power cord from the shipping bag and plug the female end into the receptacle located near the lower left-rear of the unit as seen from behind (see figure 2-1.) Make sure that the power available matches the requirements of the unit (see Power Requirements.) Set the Power ON/OFF switch at the lower left-rear of the unit to OFF and plug the power cord into an outlet.

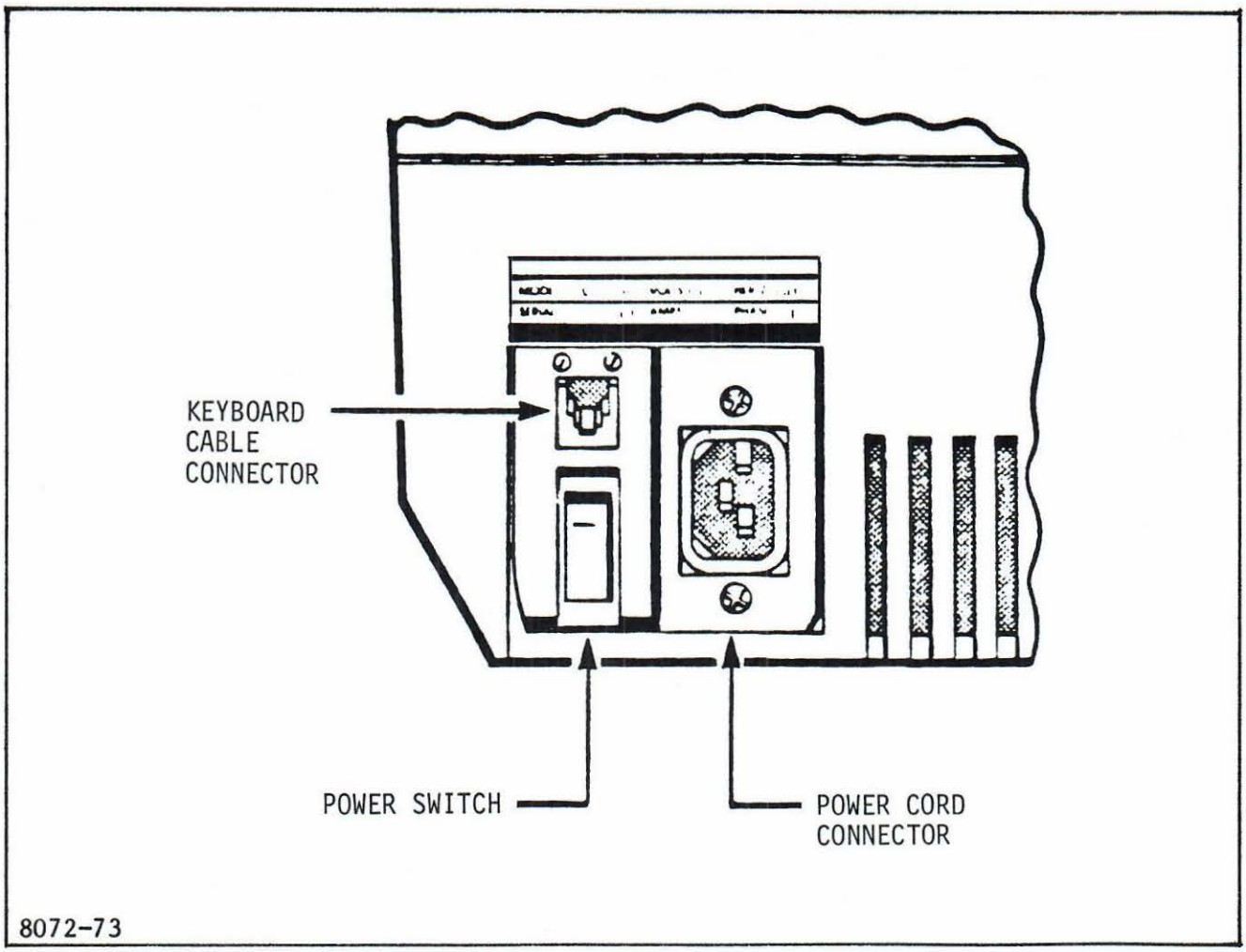

Figure 2-1. Left Rear View

6. Connect the S/10 auxiliary I/O port to your printer. The auxiliary port is the leftmost connector on the lower righthand side of the terminal as viewed from the back (see figure 2-2). The port requires a male 25 pin D connector which complies with EIA specification RS-232C.

7. (Optional) Connect the terminal's main I/O port to your host computer. The main port is located to the right of the auxiliary port. Again, a male 25 pin D connector is required.
an adapter.

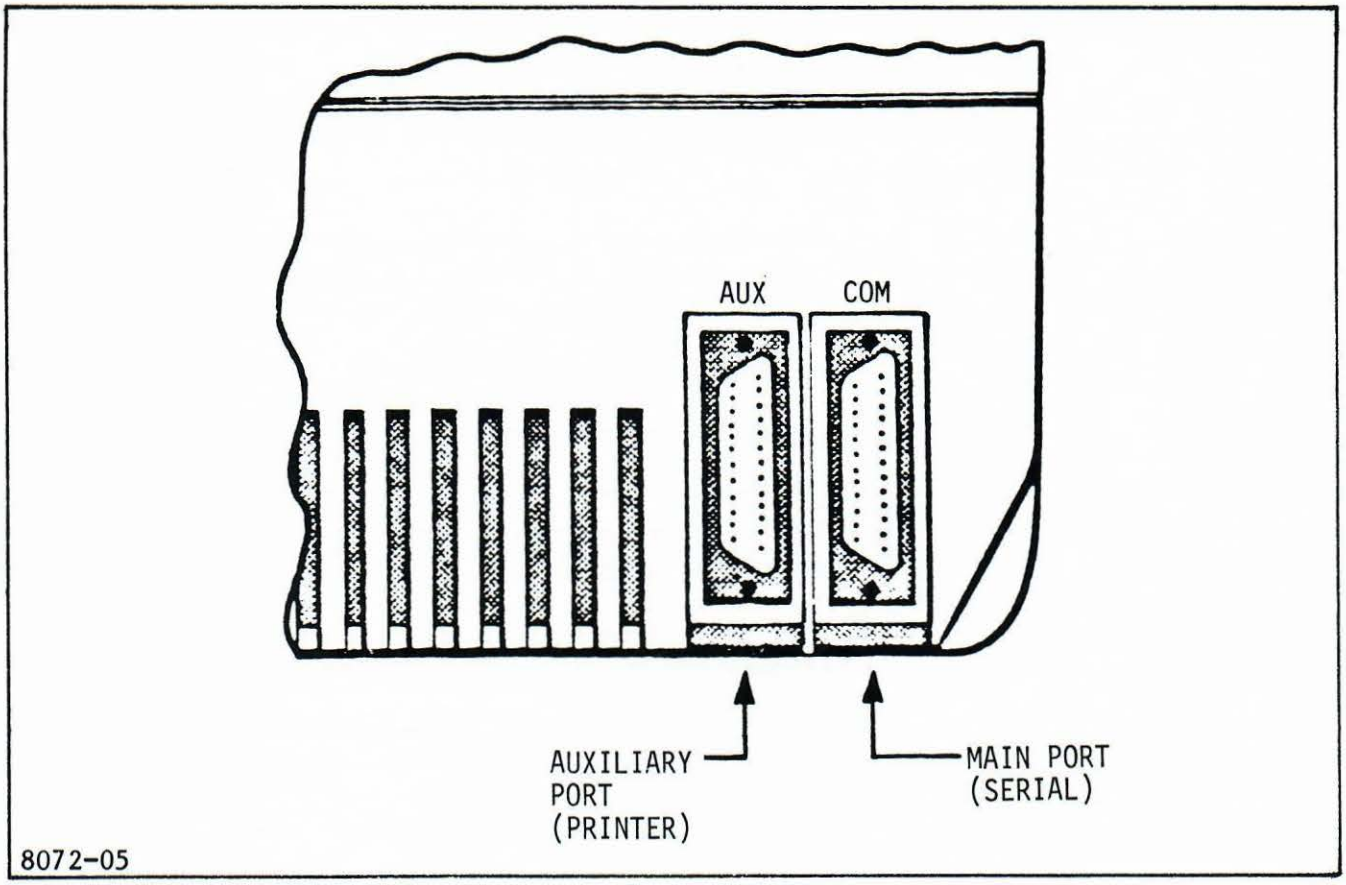

Figure 2-2. Right Rear View

2.5.1 Attaching and Detaching the Keyboard

CAUTION

Whenever the keyboard is being lowered into position, make sure that it does not fall into place. After unlatching the keyboard, it should be gently lowered into place. This should avoid damage to the keyboard.

The separate keyboard is attached to the unit by holding it perpendicular to the screen and aligning the hinge pins with the hinge holes, then pressing the hinge knobs until the pins are completely inserted into the hinges. When not in use, the keyboard may be raised and latched by turning the latch knob counterclockwise while the keyboard is in the up position. When raising the keyboard, do not slam it into place. This will avoid damage to the disk drives.

The keyboard is detached by holding it while turning the latch knob clockwise, then gently lowering it until it is perpendicular with the screen and pressing on the hinge knobs to the outside until the hinge pins release and the keyboard is freed. You may now move the keyboard to any convenient location within the length of the cord.

2.5.2 Serial Port Interface

Table 2-1 gives information required to interface a host computer or a modem to the serial port. Use of the IOMAP program enables the port assignment to be made from the keyboard.

The S/10 has full duplex asynchronous communication lines which terminate in a 25-pin connector, in compliance with all the EIA RS-232C standards. Table 2-2 gives information required to interface a printer to the Auxiliary Port.

Table 2-1. Main Serial Port Pin Assignments

PIN	SIGNAL	DESCRIPTION
1	Protective Ground (FG)	This is chassis ground, and is not to be used for reference ground.
2	Transmitted Data (TD)	S/10 origin; ASCII data output. When idle, held in MARK state.
3	Received Data (RD)	External Origin; ASCII data. Receives serially encoded data generated by the user.
4	Request-To-Send (RTS)	S/10 origin; asserted when power is ON.
5	Clear-To-Send (CTS)	External origin; asserted when connected.
6	Data-Set Ready (DSR)	Not used. (If connected, this pin must be asserted for unit to receive data).
7	Signal Ground (SG)	Common ground reference potential for all voltages on the interface. This is permanently connected to the signal and chassis ground.
8	Not Used	
9	-12VDC	Negative DC Test Voltage (unit origin)
10	+12VDC	Positive DC Test Voltage (unit origin)
11-19	Not Used	
20	Data Terminal Ready (DTR)	Unit Origin; asserted when power is ON, unless the unit is in Local Mode or the FUNCTION/TAB key is pressed.
21-22	Not Used	
23	+5VDC	Unit Origin
24-25	Not Used	

Table 2-2. Auxiliary Port Pin Assignments

PIN	SIGNAL	DESCRIPTION
1	Protective Ground (FG)	This is chassis ground; not to be used for signal reference ground.
2	Received Data (RD)	External Origin; ASCII data received from Auxiliary unit. When idle, should be held in mark state.
3	Transmitted Data (TD)	Unit Origin; used to transmit serially encoded ASCII data to the auxiliary unit.
4	Request-To-Send (RTS)	External Origin; must be asserted to receive data from auxiliary device.
5	Data Terminal Ready (DTR)	Unit Origin; asserted when power is ON, unless the unit is in the Local Mode, the FUNCTION/TAB key is pressed, or the DTR handshake Protocol is selected.
6	Not Used	
7	Signal Ground (SG)	The common ground reference potential for all voltages on the interface. This is permanently connected to the signal and chassis ground.
8	Data Carrier Detect	Unit Origin; always asserted when power is ON.
9	-12VDC (See note)	Unit Origin; negative DC Test Voltage
10	+12VDC (See note)	Unit Origin; positive DC Test Voltage

NOTE

May be used to provide signals not provided by the unit or by the attached equipment. Not intended to provide operating power for external equipment.

Table 2-2. Auxiliary Port Pin Assignments (continued)

PIN	SIGNAL	DESCRIPTION
11-14	Not Used	
15	Transmit Clock (TC)	Unit Origin.
17	Receive Clock (RC)	Unit Origin.
16,18, 19	Not Used	
20	Clear-To-Send (CTS)	External Origin; must be asserted when connected to send data out on Pin 3.
21-22	Not Used	
23	+5VDC	Unit Origin.
24-25	Not Used	

2.6 OPERATIONAL FUNCTIONS

The keyboard is the operator's primary means of communicating with the central processor, the screen, the disk drives, the printer, and the host computer. Instructions typed at the keyboard command these devices to perform various functions. When keys are depressed, codes are transmitted to the central processing unit, which interprets their meanings and performs a function or displays a character on the screen.

The Standard keyboard is similar in layout and touch to most common office typewriters. The operating characteristics are also similar to those of a typewriter. Other keys not found on a typewriter are included for data processing functions; the use of these keys is the subject of the following paragraphs.

The new International keyboard is described in paragraph 2.6.7.

2.6.1 Standard Keyboard Layout

Figure 2-3 illustrates the layout of the Standard keyboard. There are four basic groups of keys. They are:

- Main Key Group

  This group includes the characters of a typewriter keyboard, laid out in a similar arrangement, and some additional keys. It is used to enter commands and data into memory.

- Auxiliary Pad Group

  This group is laid out like a ten-key adding machine keypad and is used for numeric data entry and for some special functions.

- Motor Bar Group

  This group, located above the numeric pad, is used to control the movement of the cursor and to display the desired portion of the text in display memory on the screen.

- Function Key Group

  These keys can be programmed by the operator as described in the Operators Guide.

2.6.2 Key Combinations

The S/10 keyboard can perform many more activities than a typewriter keyboard. To avoid the confusion of an unreasonably large number of keys, the S/10 uses combinations of two or more keys for many functions. These are referred to as key combinations and are printed with a slash (/) between the names of the keys, such as FUNCTION/5. Key combinations are typed by holding down the first key or keys and typing the last key, just as a typewriter shift key is held down to type uppercase letters (e.g., SHIFT/A to type A). For example, to type the FUNCTION/5 key combination, you would hold down the FUNCTION key and simultaneously strike the 5 key.

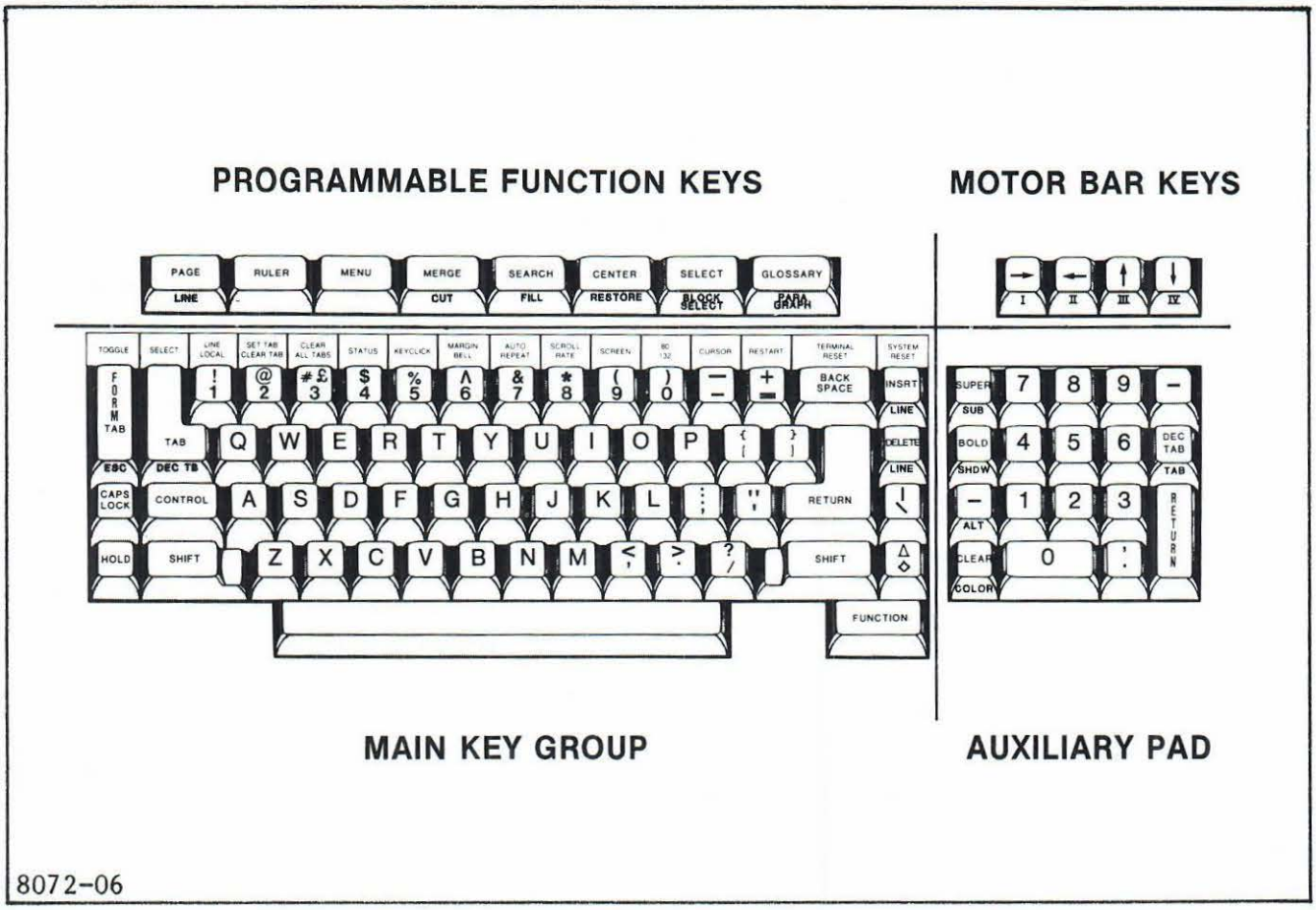

Figure 2-3. ODT and S/10 Keyboard (Standard)

2.6.3 The Main Key Group

This group includes all of the alphabetic, numeric and symbol keys, as well as several non-printing characters which are used for special purposes. These keys are similar in operation to a typewriter.

Several keys in this group perform special functions. Each of these keys is described in the following paragraphs.

SHIFT - The SHIFT key on the S/10 functions like the shift key of a typewriter. It generates no printing or nonprinting characters by itself. When pressed, it enables the uppercase function of the character set group keys. If there is no associated uppercase character, the SHIFT key has no effect.

CAPS LOCK - This key is similar to the shift lock on a typewriter; it makes all the alphabetic keys produce uppercase letters. Unlike a typewriter shift lock, CAPS LOCK does not affect the numeric and special character keys, which are shifted only with the SHIFT key. This is useful for communicating with host computer systems which do not accept lowercase letters. To remove the lock, press CAPS LOCK a second time (not SHIFT as on a typewriter).

BACKSPACE - Use of this key moves the cursor one position to the left and erases text as it moves.

HOLD - The HOLD key is used to stop and restart transmissions from the S/10 CPU or host computer. When first pressed, the HOLD key transmits an XOFF code to stop the transmission of data from the CPU to host computer. When pressed a second time, it transmits an XON code to restart the transmission of data. Check the operating procedures for your host computer to ensure that it recognizes the function of this key.

CONTROL (CTL) - This key is held down while another key is pressed to transmit a control code. Control codes are used to signal the unit to perform special functions.

SPACE BAR - Moves the cursor to the right one space at a time, similar to the space bar on a typewriter.

FUNCTION - This key is used to allow other keys to perform set up and control functions.

Several other keys are reserved for special features according to individual programs. Refer to the particular software documentation for instructions.

2.6.4 The Auxiliary Pad Group

To the right of the main character keys is the Auxiliary pad. Its layout is similar to that of a 10-key adding machine with several additonal keys. These keys enter numeric data or perform special functions for printing, host computer communications, and display manipulations.

The numeral keys, like the numeral keys in the main key group, type a numeral. These keys are also used with other keys for special functions, which are described in your software application literature.

Often the Return key functions the same as the Return key in the main key group, sometimes the Return key has a special function according to the operating program system used.

The comma/period key, used alone, types a period; used with the Shift key, it types a comma.

Pressing the 9 and Function keys, together, transmits the screen display to a printer.

The other keys in the Auxiliary pad may have special functions according to the program you are running. Some of these special functions are summarized below:

FUNCTION	METHOD
Erase Line:	FUNCTION/6 (Aux. pad) erases from cursor to end of line.
Erase Page:	FUNCTION/3 (Aux. pad) erases from cursor to end of screen.
Insert Character Mode:	FUNCTION/1 (Aux. pad) turns mode on and off; when on, characters typed are inserted at cursor.
Insert Line:	FUNCTION/4 (Aux. pad) inserts line above cursor line.
Delete Character:	FUNCTION/2 (Aux. pad) deletes character at cursor.
Delete Line:	FUNCTION/5 (Aux. pad) deletes cursor line.

2.6.5 The Motor Bar Group

This group of keys lets you control the movement of the cursor on the screen and select portions of text in memory for display. The arrows on the keys indicate the direction of cursor movement. Each depression of a key moves the cursor one character position in the direction indicated. If the key is depressed and held down with the Auto Repeat feature selected, the action is repeated until the key is released.

The third and fourth motor bar keys, MBIII and MBIV, make the S/10 screen brigher or dimmer.* The MB keys have other functions according to the program you are running. (Motor bar keys are sometimes called cursor keys.)

1. To brighten the screen intensity, press at the same time MBIII and the Control key. Pressing these two keys again brightens the screen more, one level at a time.

2. To dim screen intensity, press MBIV and the Control key. This dims the intensity one level at a time.

3. Other uses for the MB keys depend on the personality of the program that you are running. Check your software documentation for more information.

*In some S/10 models, motor bar keys I and II are used for this function.

2.6.6 The Function Key Group

The Programmable Function (PF) keys are the eight large keys along the top of the keyboard. These keys can be set by the S/10, a host computer, or the operator to send sequences of characters that are often used. By using the PF keys alone and with the Shift key, a total of sixteen sequences can be set up.

Each PF key has one or two default functions, which are applicable according to the program you are using. The labels on the PF keys describe the default functions.

Some of the programs you may also set the PF keys. The program may display labels indicating the function for various PF keys. Often the keys are referenced by numerals: from left to right, PF 1 to PF 8.

1. To set a PF key, first put the S/10 into Local Mode.

2. Signal the S/10 that you are going to set a PF key by pressing, one after the other and with no spaces or commas between, the Escape key, P, + (for ANSI mode) or the Escape key, p, + (for 7270 mode).

3. Type an attribute specifier:

   Transmit only. The key function is sent to the CPU or host computer and is not used as a terminal control sequence.

   Execute only. The key function will affect only the display memory or terminal functioning and is not transmitted to the CPU or host computer.

   Transmit and execute. The key function performs both of the above.

4. Specify which key you are setting, and whether it is to function with or without the Shift key, by typing a letter or numeral:

PF1 = 0	PF1/Shift = 8
PF2 = 1	PF2/Shift = 9
PF3 = 2	PF3/Shift = A
PF4 = 3	PF4/Shift = B
PF5 = 4	PF5/Shift = C
PF6 = 5	PF6/Shift = D
PF7 = 6	PF7/Shift = E
PF8 = 7	PF8/Shift = F

5. You can now enter a string of up to 230 characters. To enter control characters, place the unit into Monitor Mode, type the keys, and exit Monitor Mode.

6. After you have entered the string of characters that will be the function for the selected PF key, signal you are finished by pressing the Escape key and then the backslash key (the key next to the Return key).

7. The contents of PF keys are not saved in nonvolatile memory when a Save is performed. Turning the unit off or performing a reset returns their functions to the default values.

8. Following is an example of setting a PF key. After performing this setup, when PF 1 is pressed, with the S/10 in Local Mode, the word BLINK will appear, blinking.

9. While in Local Mode, press the following keys; do not space between any of the keys:

Escape Key P + 10	Attribute specifier and key selected.
Function key with M	Enter Monitor Mode.
Escape key 5m	Blinking command.
BLINK	Word to be displayed.
Function key with M Escape key	Exit Monitor Mode.
\	Ending Setup.

10. Now press PF 1, while in Local Mode, to see your PF key setup. Turning off the unit or performing a reset will eliminate the setup.

2.6.7 International Keyboard

The later model S/10 systems (Phase II) are provided with the International keyboard. Figure 2-4 illustrates the International keyboard. Most functions of the International keyboard are the same as the earlier model Standard keyboard. Additional keys and functions have been added to the International keyboard and are described below. See previous paragraphs for Standard key descriptions.

AUX CHR (Main Key Group) - Enables the use of auxiliary foreign language characters. There are two sets of foreign language characters: the International Standards Organization Character set (ISO) and the Basic Four® World Trade Character set (B4). The ISO set includes characters for Spanish/Puerto Rican, Norwegian, Italian, Swedish, Portuguese, Germain, French. This set also includes characters used in the United Kingdom. The B4 set includes characters for French; French Belgian; Danish; Austrian/German; Italian/United Kingdom; Finnish/Swedish; Portuguese; Spanish/Puerto Rican; and Norwegian.

To access foreign language characters refer to operators manual.

NUL/DEL (Main Key Group) - This key sends an ASCII delete (DEL). If pressed with the SHIFT key, it sends an ASCII NULL (NUL).

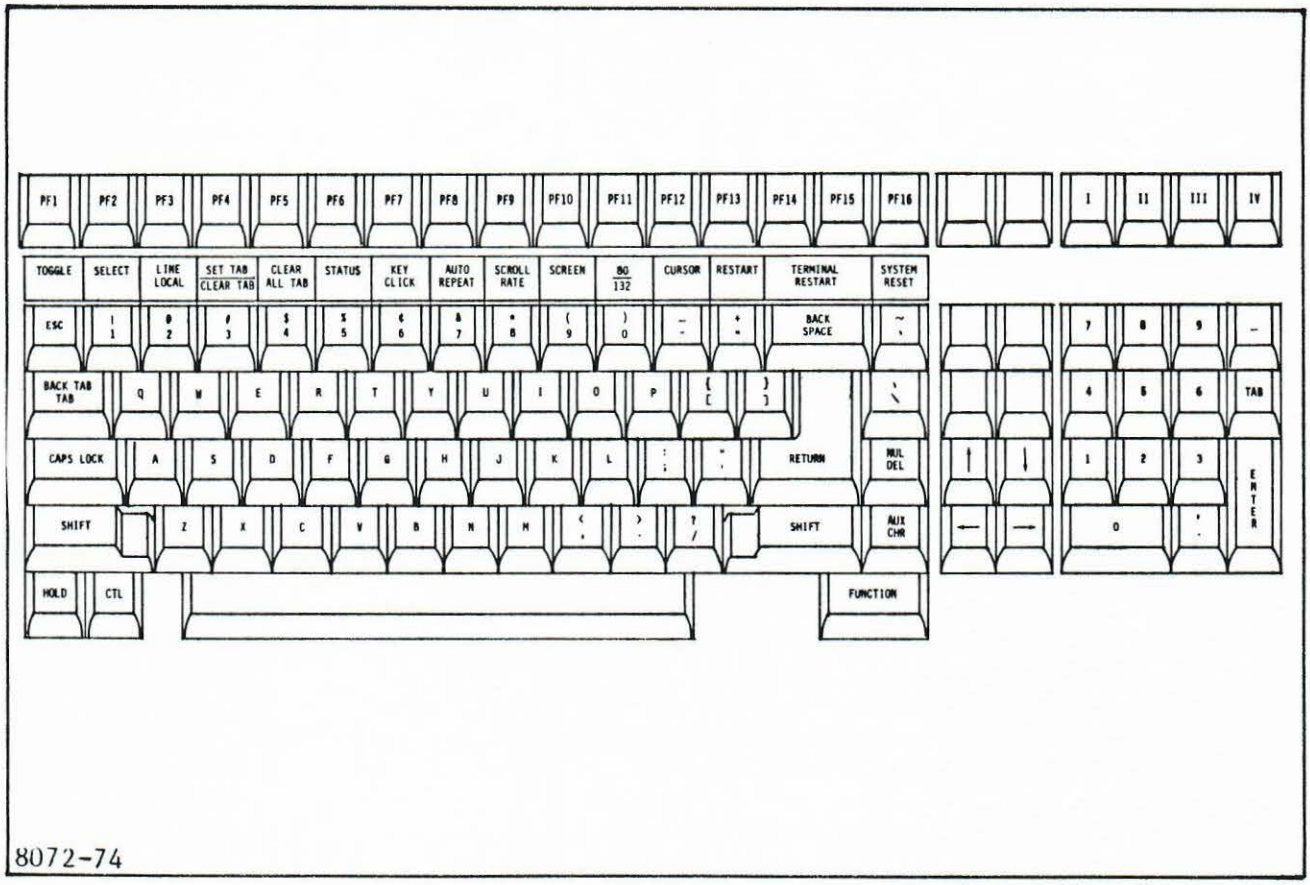

Figure 2-4. ODT - S/10 Keyboard (International)

BACK TAB/TAB (Main Key Group) - This key works like the tab key on a typewriter. It moves the cursor to the next tab stop to the right of its current position. If there are no tab stops set, the cursor moves to the right margin. Instructions for setting and clearing tabstops are in the next section.

PROGRAMMABLE FUNCTION KEYS (PF1 - PF16) - The keys above the main key group are Programmable Function keys and are often referenced by numerals from left to right, PF1 to PF16. However, there are an additional 22 keys on the keyboard (with other names) that are also Programmable Function keys. You can use all 38 of these keys several different ways.

The Programmable Function (PF) keys can be set by the S/10, a host computer, or the operator to send sequences of characters that are used often. By using the PF keys in combination with either the SHIFT key, the CONTROL key, or with both the CONTROL and SHIFT keys, you can set up a total of 147 sequences.

Some of the programs you use may also set the PF keys. The program may display labels indicating the function for various PF keys.

1. To set a PF key, put the S/10 into Local Mode.

2. Siganl the S/10 that you are going to set a PF key.

   a. Press the ESCAPE key, P, + (for ANSI Mode)

   or

   b. Press the ESCAPE key, p, + (for 77270 Mode).

   Do not type the commas or leave any blank spaces when entering your option.

3. Type an attribute specifier:

   Transmit only. The key function is sent to the CPU or host computer and is not used as a terminal control sequence.

   Execute only. The key function affects only the display memory or terminal functioning and is not transmitted to the CPU or host computer.

   Transmit and execute. The key function performs both of the above.

4. Specify which key you are setting and whether you want it to function without any special keys, with the SHIFT key, with the CONTROL key, or with the CONTROL and SHIFT keys. You can program most keys up to four levels. However, the ESCAPE key, the TAB key, the SPACE BAR, the RETURN key, and the BACKSPACE key are programmable to three levels only.

	SEQUENCE SPECIFIERS	KEY SPECIFIERS		
	ALONE	SHIFT	CONTROL	SHIFT AND CONTROL
PF1	+ 0	6	G	O
PF2	+ 1	9	H	P
PF3	+ 2	A	I	Q
PF4	+ 3	B	J	R
PF5	+ 4	C	K	S
PF6	+ 5	D	L	T
PF7	+ 6	E	M	U
PF8	+ 7	F	N	V
PF9	- 0	8	G	O
PF10	- 1	9	H	P
PF11	- 2	A	I	Q
PF12	- 3	B	J	R
PF13	- 4	C	K	S
PF14	- 5	D	L	T
PF15	- 6	E	M	U
PF16	- 7	F	N	V
Motorbar I	m 0	8	G	O
Motorbar II	m 1	9	H	P
Motorbar III	m 2	A	I	Q
Motorbar IV	m 3	B	J	R
Main Key Cursor				
Escape Key	q	8	G	O
Back Tab/Tab	q	9	H	P
Space Bar	q	A	I	Q
Return Key	q	B	J	T
Backspace Key	q	C	K	S
Auxiliary Keypad				
Return Key	q5	D	L	T
Tab Key	q6	E	M	U
- Key	q7	F	N	V
Cursor/Screen Keys				
Cursor Left	c 0	8	G	O
Cursor Right	c 1	9	H	P
Cursor Up	c 2	A	I	Q
Cursor Down	c 3	B	J	R
Cursor Blank (L)	c 4	C	K	S
Cursor Blank (R)	c 5	D	L	T
Screen Brighter	c 6	E	M	U
Screen Dimmer	c 7	F	N	V
Clear Screen	a 0	8	G	O
Clear Foreground	a 1	9	G	P

5. Enter a string of up to 80 characters.

6. After you enter the string of characters that will be the function for the selected PF key, signal that you are finished by pressing the ESCAPE key and then the BACKSLASH key (the key next to the RETURN Key).

   The set functions of PF keys are not saved in nonvolatile memory when a Save is performed. Turning the unit off or performing a reset returns their functions to the default values.

MOTOR BAR KEYS - The Motor bar keys on the International keyboard do not contain the cursor control keys as with the Standard keyboard.

The four Motor bar keys are located at the top right of the keyboard In 7270 Mode, the Motor bar keys generate field separator (I), group separator (II), record separator (III) and unit separator (IV) control characters. In some software applications, the Motor bar keys have different functions. See your specific software literature for an explanation of those functions.

AUXILIARY KEYPAD - The numeral keys, the RETURN key, and the TAB key function the same as their counterparts in the main key group when pressed alone. However, when you press them at the same time as the FUNCTION key, each carries out a new action.

FUNCTION and 1 - Using these keys together inserts one blank space to the left of the cursor. Characters to the right of the cursor move one space to the right.

NOTE

When in ANSI Mode, prressing FUNCTION and 1 enables the Insert Character Mode. This mode lets you insert the desired character at the cursor. No space is inserted. Press the FUNCTION and 1 keys again to disable the Insert Character Mode.

FUNCTION and 2 - This combination deletes the character at the cursor position. Characters to the right of the cursor move one space to the left to fill the space.

FUNCTION and 3 - Using these keys together erases text from the cursor to the end of the screen.

FUNCTION and 4 - This combination inserts one blank line above the cursor. Characters on the cursor line move down one line.

FUNCTION and 5 - This combination deletes the line the cursor is on. Lines below move up one line to fill the space.

FUNCTION and 6 - Using these keys together erases text from the cursor to the end of that line.

FUNCTION and 7 - This combination moves the cursor to the home position of the active scrolling region when you are in Origin Mode. If no scrolling region is set, the cursor moves to the upper left corner of the screen.

NOTE

The scrolling region is that part of the screen that you can scroll while the rest of screen remains stationary.

FUNCTION and 8 - This combination transmits all subsequent entries on the screen to the printer.

FUNCTION and 9 - This combination transmits the screen display to a printer.

FUNCTION and - (minus sign) - Using these keys together transmits a long break signal (3.5 seconds).

FUNCTION and TAB - Using these keys together transmits a short break signal (.275 seconds).

FUNCTION and ENTER - This combination transmits the answer-back message.

CURSOR KEYPAD KEYS - The Cursor Control keys are between the main key cluster and the Auxiliary keypad. These six keys control cursor movement and screen brightness.

The Cursor Control keys perform the movements shown on the keys when you press them alone. However, if you press them at the same time as you press the FUNCTION key, they perform different movements.

Cursor Up - This key moves the cursor up one line. If you press this key in combination with the FUNCTION key, the active scrolling region moves up one line.

Cursor Down - This key moves the cursor down one line. If you press this key with the FUNCTION key, the active scrolling region moves down one line.

Cursor Right - Thie key moves the cursor one space to the right. If you press this key with the FUNCITON key, the next page of your document displays.

Cursor Left - CURSOR LEFT moves the cursor one space to the left, if you press this key with the FUNCTION key, the previous page of your document displays.

Brighter (Top Left) - This key, in increments, increases screen brightness each time you press this key with the FUNCTION key.

Dimmer (Top Right) - This key, in increments, decreases screen brightness each time you press this key with the FUNCTION key.

CURSOR AUXILIARY KEYS - The Cursor Auxiliary keys are the two dark keys directly above the Cursor keypad. They are between the PF keys and the Motor bar keys.

When the S/10 is in 7270 Mode, these keys do the following:

Left Key - This key clears the screen, deleting displayed data. You must press the FUNCTION key at the same time.

Right Key - This key clears all bold characters from the screen. To do this, you must press the FUNCTION key.

2.7 USE AND CARE OF DISK AND DRIVE

The S/10 has two 5 1/4-inch floppy disk drives mounted one above the other to the right of the screen. The double sided drive has approximately 62.2K bytes of double sided, double density storage per drive.

The standard drives use double sided, double density, soft sector diskettes. All diskettes must have center reinforcements. BFISD recommends that only diskettes from the following manufacturers be used for optimum performance and data integrity:

Manufacturer	Double-Sided
Dysan	No. 204/2D
Verbatim	No. MD 577-01-18212

The unit is shipped with one disk containing a copy of the BBM/CPM operating system and the following files:

FILENAME	PURPOSE
0A1000.TRM	Default terminal personality
TXFER.COM	Personality load program
SYSGEN.COM	CP/M copy utility
FORMAT.COM	Disk format/verify utility
COPY.COM	File copy utility
BACKUP.COM	Disk copy utility
STAT.COM	File size/status utility
HELP.COM and related files	Operator Help System
DEMO.COM and related files	Demonstration Programs

2.7.1 Disk Insertion

Disks are inserted in the drives with the label side facing up and the large rectangular notch facing to the left, as illustrated in figure 2-5. Gently place the disk as far into the drive as it will go. Be careful to insert the disks only in this manner to avoid damage, and always check to be sure the drive is empty before inserting a disk.

Disks should never be inserted in the drives when the power is not on, nor should the power be turned off when disks are in the drives. Turning the power on and off with disks in the drives can result in damage to the disks and loss of data.

When changing disks during use, remove the current disk first, type the command to access the new disk (often CONTROL/C), then insert the new disk. This prevents damage to the center of the disk.

A few simple precautions should be taken in handling floppy disks to avoid damage. They should be treated with the same care you would give to other recording media such as phonograph records or recording tape. Handle them gently at all times, and do not touch the brown disk surface. Do not let them come in contact with liquids, ashes, paperclips, or anything magnetic. Don't bend them out of shape or put heavy weights on top of them. Never use ball point pens or pencils to write on the labels; mark labels before putting them on the disks or use a soft felt tip pen.

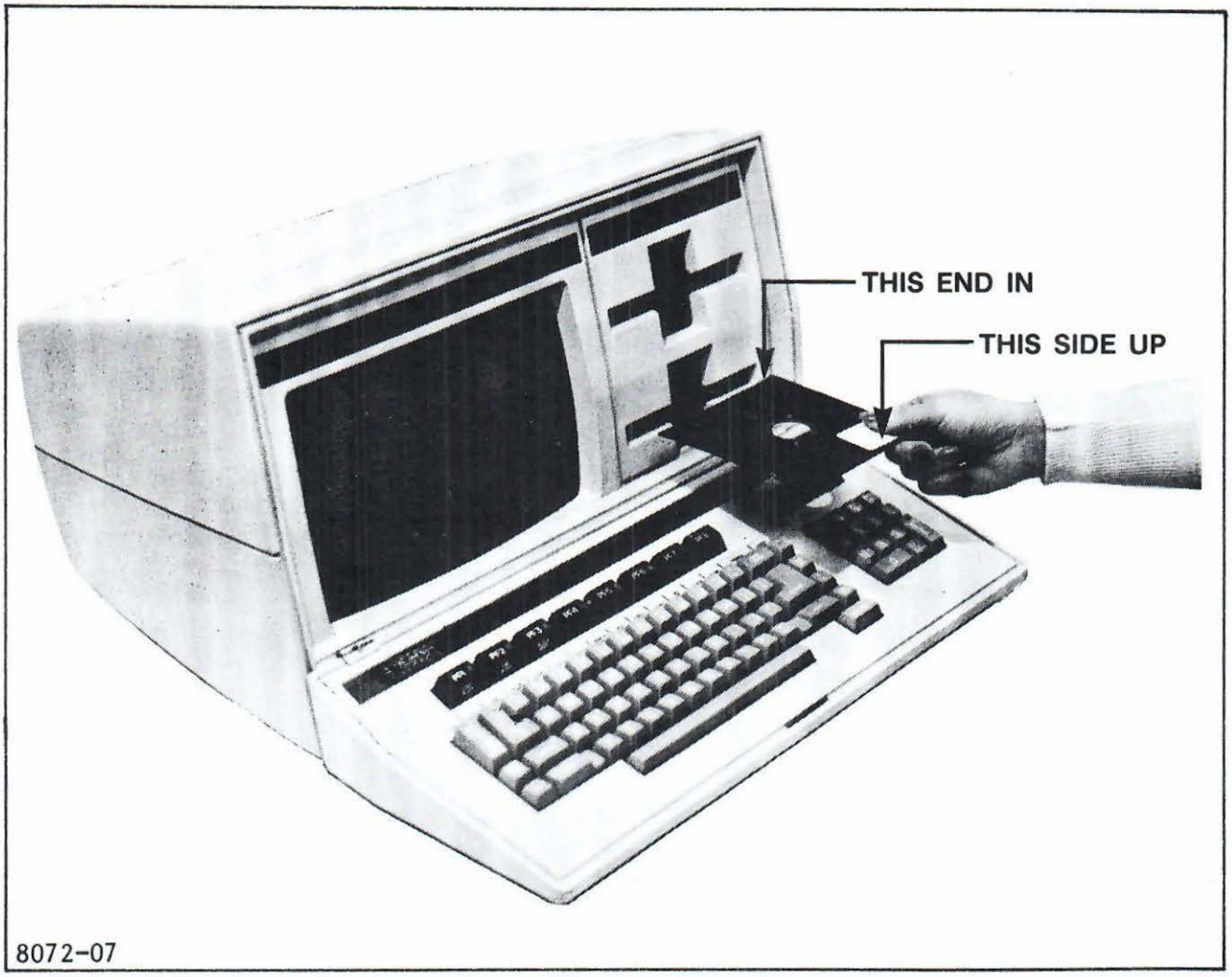

Figure 2-5. Proper Disk Insertion

Proper storage of disks is also important. Keep them in their protective jackets whenever they are not in use. Never pile disks on top of each other - instead, store them upright. The boxes in which they are packaged are good for this purpose. Your office supply vendor can provide you with excellent filing and storage containers for your disks. With proper care, you can increase the life of your disks and avoid loss of data.

It is vitally important to make backup copies of important disks, especially master disks containing copies of programs (such as the distribution disk that came with your S/10). It is a good idea to copy such disks before using them and save the master disk, using the copy as the working disk.

A few simple precautions should be taken in handling floppy disks to avoid damage. They should be treated with the same care you would give to other recording media such as phonograph records or recording tape. Handle them gently at all times, and do not touch the brown disk surface. Do not let them come in contact with liquids, ashes, paperclips, or anything magnetic. Don't bend them out of shape or put heavy weights on top of them. Never use ball point pens or pencils to write on the labels; mark labels before putting them on the disks or use a soft felt tip pen.

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It is vitally important to make backup copies of important disks, especially master disks containing copies of programs (such as the distribution disk that came with your S/10). It is a good idea to copy such disks before using them and save the master disk, using the copy as the working disk.

2.7.2 Write Protection

Each box of disks provides a sheet of 3/4 inch foil stickers. These are called write protect tapes, and are used to prevent alteration of the contents of disks. Disks that have been write protected can be read by the drives, but no changes can be made or new data added. One use of this feature is to protect backup copies of software or data. It is a good idea to write protect a master disk (such as the distribution disk) after making a backup copy. If the working copies are lost or damaged, you can make a copy from the backup, but the backup cannot be inadvertently erased or altered.

To write protect a disk, fold a write protect tape over the large rectangular notch, being sure that the entire notch is covered and the fold lines up with the edge of the disk. When write protection is no longer desired, simply peel away the tape.

2.8 RESETTING THE S/10

There are three ways to reset the S/10. Resetting lets you start over again if you encounter difficulty or you want to use a different program. None of the three resets can cause any damage to your data and programs if they are recorded on disk.

The first reset clears S/10 screen and display memory, restores the saved configuration settings, and runs the self tests. The operating system and any programs that have been loaded into the unit are not affected. However, if you are communicating with a host computer, you may have to start over again. This reset is accomplished by holding down the FUNCTION key and pressing TERMINAL RESET (BACKSPACE key).

The second reset causes an operating system cold start (boot). This reset clears any programs and data from main memory and restores the operating system prompt. Display memory is not cleared, and the screen display also may not be cleared. To boot the operating system, hold down the FUNCTION key and press SYSTEM RESET (the INSRT key).

The third type is a full reset which performs the functions of the first two resets and also reloads the terminal personality into display memory. This is equivalent to starting over again by turning the power off and on again, but it causes less wear on the components. To fully reset the unit, hold down the FUNCTION key and press RESTART (the + = key).

SECTION III

FUNCTIONAL DESCRIPTION

3.1 INTRODUCTION

This section describes the functional description of the Office Display Terminal (ODT) and the System S/10. It includes a description of the operating system, a description of the hardware with a block diagram, and a description of each printed board assembly, based on the schematic diagrams located in the Section VIII, Reference Data.

The information contained in this section will enable a trained service technician to understand the operation of these units. If the troubleshooting procedures indicate a fault on a printed circuit assembly, these descriptions will aid the technician in locating the fault on the board.

The electronics for the ODT are contained on the AVP board, shown on the schematic 051280 Sheets 1-1 through 1-5 in the Reference Data. The additional circuits required for the S/10 are on the Advanced Floppy Controller board, and are shown on schematic 051300 Sheets 2-1 through 2-3. The Reference Data also contains schematics for the Motherboard and Power Supply assemblies.

Technical and servicing information regarding the Video Electronics and CRT Display, the 96 TPI Disk Drives and the Disk Floppy Disk Formatter/Controller are located in Section VIII, Reference Data Section.

NOTE

> This section assumes that the unit is operating under the standard terminal personality. Other personalities differ in the software aspects of their operation. The standard personality should always be used when servicing a unit.

3.2 OPERATION OF THE OFFICE DISPLAY TERMINAL (ODT)

The Office Display Terminal (ODT) include a keyboard for data entry, a CRT for display, and two serial I/O ports which transmit and receive data between a host computer, a printer, or a modem to a telephone line. Each of these ports has full transmit and receive capability, so that all protocol between the host computer and the terminal can be observed, and all format and spacing features of the printer can be fully utilized.

Terminal personalities can be loaded into the EPROMs to allow the terminal to interface with a specific computer.

The ODT has a Z80 microprocessor designated Z80-1, which controls the I/O ports, the keyboard port, and the operation of the CRT display. The processor has a 16K (64K for S/10) byte Random Access Memory (RAM) for data storage, and a Read Only Memory (ROM) to initialize the unit at power up or reset. When the ODT is designed to interact with a specific host computer, ROM also contains the terminal personality. An additional Non-Volatile RAM (NVR) stores initialization data such as the data baud rates, screen intensity, and operator convenience features. These variable terminal features can be retained when power to the unit is turned off.

Data is moved from the RAM of Z80-1 to the Display Controller by a Direct Memory Address (DMA) circuit. Data transfers are initiated by Z80-1, then the DMA transfers the data as required by the video circuits, allowing the processor to perform other tasks. This enhances the operating speed of the terminal.

3.2.1 Display Characters

The font memory has 256 character positions comprising two completed 128 character fonts; each character comprises 96 bits arranged into twelve bytes. In the standard arrangement, each character is a 7x12 dot matrix in a 10x12 dot field. The most significant seven data bits for each row have a "1" representing a dot and a "0" when the dot is off. The least significant bit, when set, indicates that the entire row is displayed with a half-dot shift to the left, which permits a better proportioned display for certain characters. A half-dot shift does not operate on the initial dot in the raster.

Figure 3-1 shows the construction of a standard 80-column character. Each character is followed by three dots that are off (unless the character is used for graphics).

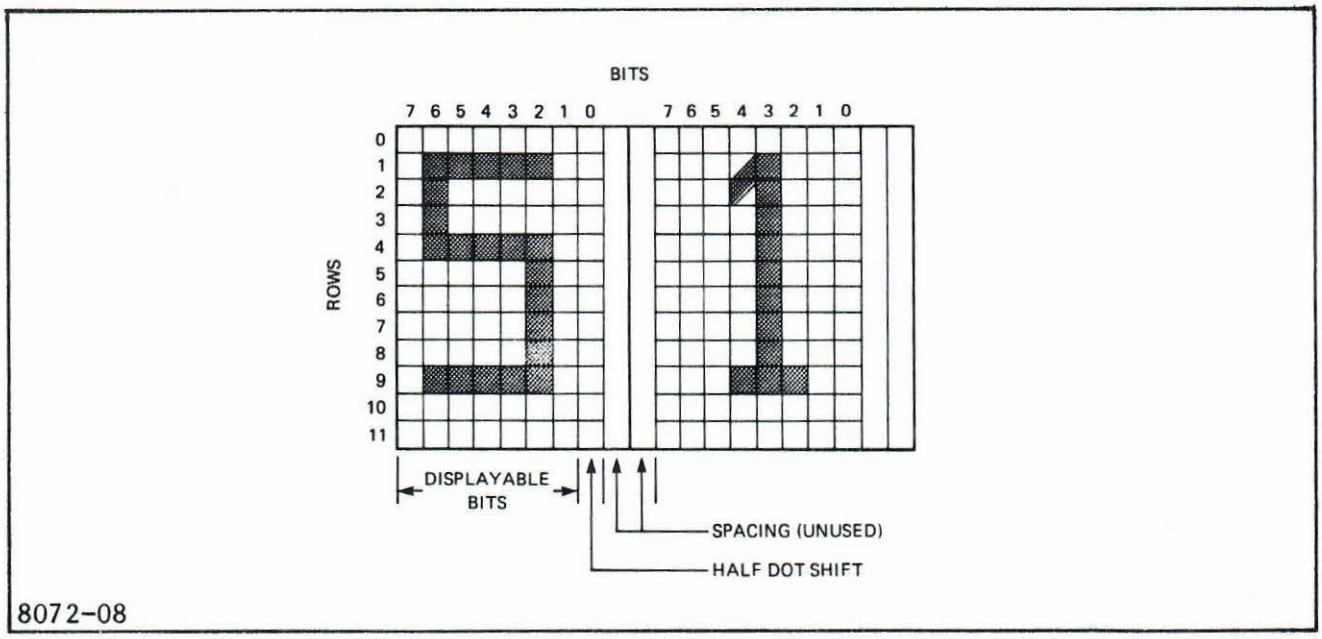


Figure 3-1. 80 Column Format

For special graphics characters, the most significant bits of each row are displayed as in the standard character, and bit 0 is again a half dot shift (if set). Bits 1 and 2 control the three dots to the right of the field, shown in figure 3-2. The data format is as follows:

BITS	DISPLAY	BITS	DISPLAY		
00	ooooo	10	*oooo	where	*=ON
01	o*ooo	11	*****		o=OFF

This allows continuous lines to be formed across the display when bits 1 and 2 are both "1".

When the 132-column display mode is selected, shown in figure 3-3, each character is displayed with 6x10 dots in a 6x12 field. The six most significant bits of each row contain the dots for that row, and the least significant bit indicates the half dot left when set. There is no need for special treatment for graphics.

The 80-column display has 24 character lines of 12 rasters each, with a 25th line for the status display. When the 132 column display is selected, 24 character lines of 12 rasters each are used, with Line 25 as the Status Line. If 28 character lines are selected, there are 10 raster lines to each line, with the status line as line 29. The top raster line is normally blank for interline spacing. In the terminology used in this manual and on the schematics, the status line is always referred to as line 25. The raster lines are in effect the character generator address. Figure 3-4 shows the raster line assignment for the 80- and 132-column modes (24 or 28 character lines), and the position of the upper and lower case, the "i" dot, the descender and underscore.

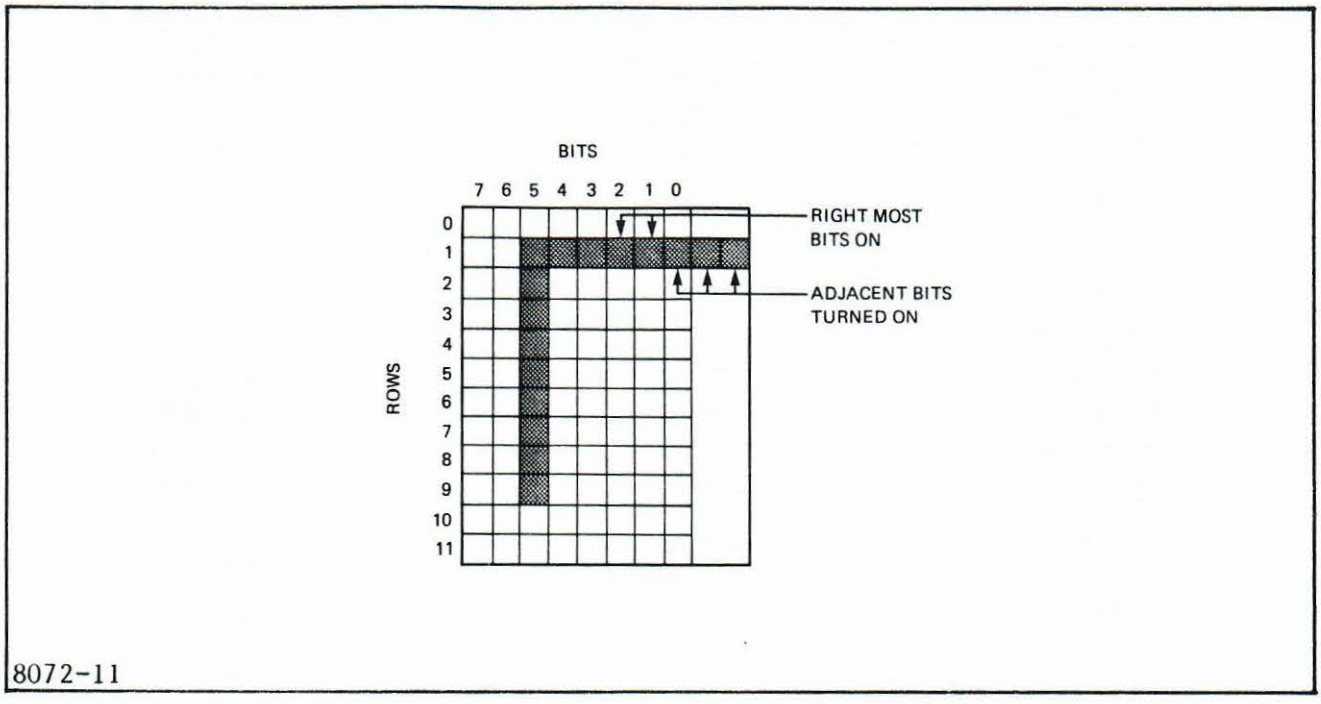


Figure 3-2. Special Graphics in the 80 Column Mode

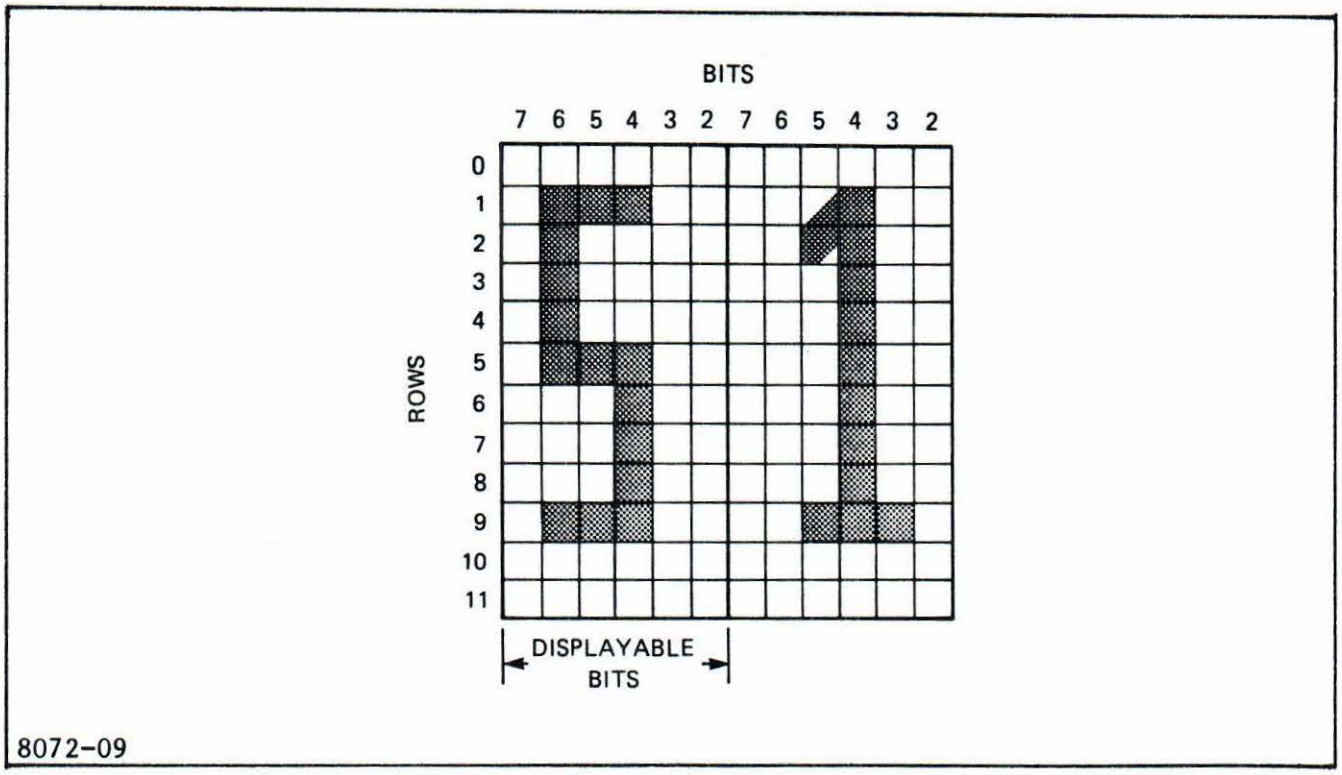


Figure 3-3. The 132 Column Font

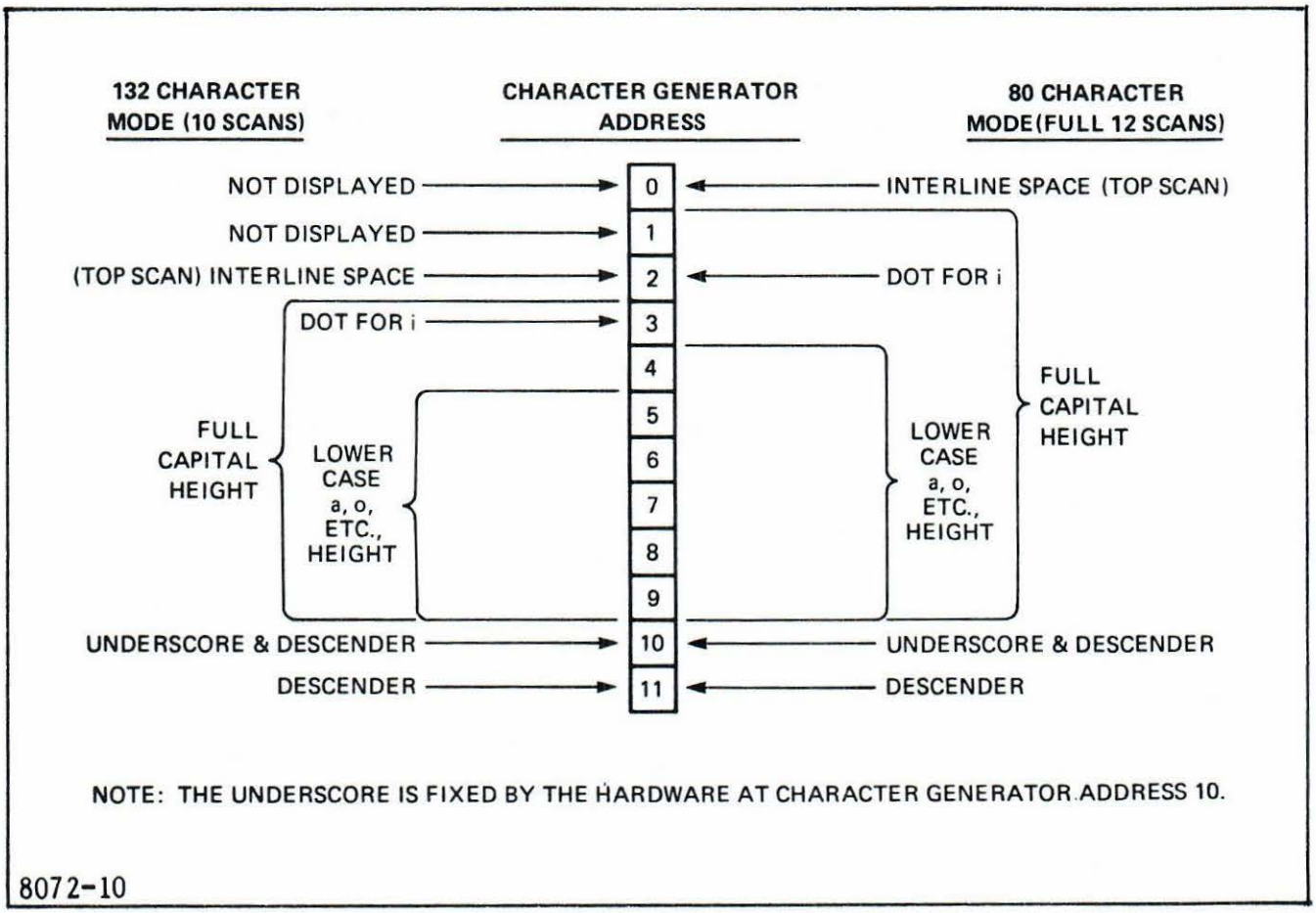


Figure 3-4. Address Assignments for 80 and 132 Column Fonts

3.2.2 Video Display Data

Z80-1, the AVP microprocessor, runs at 4.6 Megahertz. Data for the display is assembled in RAM-1 from the various sources (keyboard, AFC, serial port) in preparation for display. This data is transferred thru the DMA (Direct Memory Access) into the Line Buffer without the aid of Z80-1, allowing Z80-1 to perform other functions.

The DMA has a table of commands (pointers) called the Video Display Table (VD Table), which allows display data to be stored at random locations in the RAM. The table contains the start-of-line RAM address, the number of raster lines for the character lines, and the starting raster line number for the character generator. The VDT therefore contains the entry point for each line on the screen. The first VDT entry is a two-byte memory address for the status line. Each of the following entries are four bytes each:

Byte 0 - The low order byte of the character line start address.

Byte 1 - The high order byte of the character line start address.

Byte 2 - The raster control byte.

Byte 3 - The character generator control byte.

The Raster Control Byte determines the number of raster scan lines in the display line. It is used to permit smooth scrolling by allowing the program to adjust the number of raster scan lines for the first and last lines of a scrolling region. The raster control field also permits shorter than normal height display for such applications as 28 line displays.

The Character Generator Control Byte sets various aspects of character generation and font loading. It indicates which row in the character generator to use for the first raster scan on the screen. It is incremented for each raster scan in the display line, or every other line for double-high characters. This allows any portion of the character to be displayed for smooth scrolling.

The display controller forms the display for one character line from the data from the VDT. The Raster Control Character Generator Control Byte information control the format for the line. The address for this character line is contained in the first two bytes of the VDT memory.

The character line is a data structure located randomly in memory. The data line contains data and control information for a single display line. The first byte is a cursor position byte, the second the font selection, and the third the video attribute byte. The remaining bytes are data for the line, terminated by an end-of-line code. Software constraints limit the character lines to 238 bytes, which allow six control bytes (with the EOL) and 232 character and attribute bytes.

3.2.3 Status Line

The first entry in the VDT points to the character line for the status line. This line is displayed at the bottom of the screen as line 25, or line 29 in the 132 column 28-line mode. The status line is different from a character line in the following ways. It can only display characters in the single-high mode. The first two bytes are always 00H, and are the Raster Control and Character Generator Control Bytes. The third is the cursor byte, the fourth the font selection, and the fifth the video attribute code. The remaining bytes are data for the status line, terminated by an End-of-Line code. Hardware constraints limit the status line to 232 bytes, which allow six control bytes (with the EOL) and 226 character bytes.

The status line is indicated in the system by a point designated LDST, which is the end of the tenth raster on the 24th line in the 80-column mode, or the end of the tenth raster on the 28th line in 132 column mode. The Master Clock generates a hard screen location at this point, which indicates that the line buffer must be reloaded. The line buffer is displaying line 24, and the DMA has finished loading the next line buffer memory page with the next line. Line 25 is a non-displaying line, except during smooth scroll, but it does exist in the VDT for scrolling.

The VDT has 32 lines, more lines than are normally required in the line buffer, since additional lines are required for split screen, smooth scroll, and a last dummy line for its EOL. The start of the status line is transferred by the DMA to the Line Buffer using the 2-byte status address start, first two bytes from the VDT, which the DMA stored temporarily for use at the Status Line start.

3.2.4 Loading Data Into The Line Buffer With The DMA

The display has a table-driven video system (as opposed to memory mapped) in which the character font is related to the raster scan and line elements of the display. Z80-1 provides the Display Controller with a starting address each 16.7 milliseconds. This address is the data location of the Video Display Table (VDT) in RAM-1. The VDT contains an entry for each character line on the display. The first entry is the 2-byte address for the status line, during which time Z80-1 receives an interrupt. The following entries are four bytes each for each character line, where the low order byte of the character line address is byte 0, the high order byte of the character line address is byte 1. Byte 2 is the raster control byte, and byte 3 is the character generator control byte.

The table and the lines are written in random order; the starting point of each line is addressed by the series of 4-byte groups in the Line Buffer table. Z80-1 takes the two byte VDT starting address and loads it into the DMA. The DMA uses this as the address for RAM-1, and fetches the first block of data. The data is sent to the Line Buffer in the Display Controller, which is set up such that it will receive data during DMA cycles. The DAM switches data internally when it gets the starting table address from Z80-1, so that data is written into the Line Buffer in sequence.

3.2.5 Assembling a Character Line

The Line Buffer has two halves which allow data to be loaded into one half while data previously loaded in the other half is output. These halves are swapped to continue the process of transmitting data to the display. The display controller forms a character line by reading the VDT entry for that line. Line format is set by the raster control and character control bytes. The address for the character line is contained in the first two bytes of the VDT entry.

The first byte is the cursor address; the second is the font selection. The third byte is for the video attributes, then the data bytes, which terminate in C0 to signal End of Line (EOL) to the Line Buffer. This shuts the Line Buffer transmission off, and RAM-1 refresh is begun.

3.2.6 Refresh

RAM-1 is a dynamic RAM and must be fully refreshed at intervals of 2 milliseconds. RAM-1 shares data and address buses with the DMA. Since the DMA has the function of addressing RAM-1, refresh is also part of the DMA function. During the refresh period, Z80-1 and the DMA share memory cycles. The DMA sequences through the RAM performing only refresh functions.

3.2.7 The Double-High Character Line

Double high characters are displayed using two separate display lines, one for the top half of the character, and one for the bottom half. The character generator allows up to twelve horizontal lines for each character. The top six lines are allocated to the upper character line, with each of the raster scans repeated twice, unless bit 0 is set to allow a single display for smooth scroll, and similarly for the bottom character line.

3.2.8 The Non-Volatile RAM

The Non-Volatile RAM is a memory circuit that can be updated during system operation, but retains the data when power is turned off. It has a capacity of 64 bytes, and may store any of the following functions for the standard terminal personality:

ANSI or Continous Mode
ANSI or VT52 Mode
Answerback Message
Auto Line Feed

Auto Repeat
Auto XON/XOFF
Bits per Character
Characters per Line

Cursor Key Mode
Cursor Scroll Mode
Cursor Style
Double Wide Mode

Local Echo Mode
Margin Bell
New Line Mode
Origin Mode

Parity Generated
Parity Sense
Printer Port Settings
Receive Baud Rate

Screen Background
Screen Intensity
Scroll Rate
Status Line Displayed

Erase Mode	Tabstops
Keyclick	Transmit Baud Rate
Keypd Application Mode	US or UK Character Set
Line or Local Mode	Wraparound Mode

The bytes stored vary with the personality of the unit. Consult the User's Guide for details.

3.2.9 Interrupt System

Each processor has a separate vectored interrupt system, with controllable mask and priority encoding. The 32-bit port generates an interrupt to the receiving processor whenever data is stored in the port waiting to be transferred.

Z80-1 receives an interrupt from each serial port when data is being transmitted to and from the external device. An interrupt from the master clock indicates that line 25 (the status line) is being displayed and the DMA needs a new VDT starting address.

Z80-2 (located on the Advanced Floppy Controller circuit board) is interrupted by the floppy disk controller whenever data is being written or read.

3.2.10 System Clocks

The system Master Clock generates the primary system clock frequency of 18.432 Megahertz. This is divided down and used as an input by Z80-1 and Z80-2, Video Sync, RAM-2 Refresh, and as a clock for the control circuits in the Line Buffer and Attribute Generator. The 8 Megahertz Generator and Divider for the floppy disk controller has an independent oscillator.

The Video Sync generates the following timing signals from the primary clock:

1. F/2 is used to synchronize the DMA and DMA Controller, and for RAM-1 memory timing.

2. HORIZD syncs the horizontal components of the display, and the vertical blanking.

3. Dot Rate Clock for character output timing.

4. HORIZ for horizontal sync.

5. 9.62kHz for the keyboard RS-232C port.

6. 2.2kHz for the speaker.

7. VB, Vertical Blank.

8. Beginning of Status Line.

9. Load Status Line.

10. LDST*, video refresh interrupt.

11. CLRMRG, reset line buffer to accept the first two data lines for the next video field.

3.3 OPERATION OF THE SYSTEM S/10

The S/10 unit is an ODT Terminal with the addition of a second circuit assembly called the Advanced Floppy Controller (AFC), and two floppy disk drives. Also required are additional cables, and a fan to cool the drives and circulate air. The S/10 also has larger power supply to supply the additional power required for the extra board and drives. (See figure 3-5, System Block Diagram.)

The AFC has a microprocessor, Z80-2, which is the controller for the disk drives, and runs local CP/M or BB/M-based programs. This Z80 has a dedicated 64K Random Access Memory (RAM) and communicates with Z80-1 through a 32-bit bi-directional port.

The floppy disk controller and Z80-2 provide control and interface for the two disk drives. Programs or data downloaded from a disk are stored in RAM-2, and are transferred from there, via the 32-bit port, to the Z80-1 system. The controller serializes data to be written on the disk, and converts received data to parallel format to be stored in RAM-2. It also provides control signals to the drives and receives all status indications from the disk drive. All data transmitted to and from the disk is stored in RAM-2. The disk drives are double-sided, 96 TPI. All drives use the MFM encoding method. The data capacity of the disk for each version is given in the specification.

3.3.1 The Disk Controller System

The disk controller system consists of the disk controller, a second microprocessor (Z80-2) and RAM-2, which is dedicated to servicing the floppy disk drives, running the BB/M or CP/M-based programs, and contains a boot PROM which boots up this part of the system upon initialization or reset. This system communicates with the DMA and Z80-1 via a 32-bit port.

Z80-2 is a standard processor operating at 4.6 Megahertz, with 64K of RAM and a floppy disk controller chip. The controller chip takes the command structure from Z80-2, selects the operating disk drive, positions the head over the required track, and instructs it to read or write a sector or file. All of the program to operate the controller is resident in RAM-2. The controller also receives status signals from the disk drives (index, track 0 indication, and write protect) and transmits data read from the diskette to Z80-2.

RAM-2 is a dynamic RAM, and requires a refresh circuit to refresh the RAM each 2 milliseconds.

Z80-1 and Z80-2 communicate through a 32-bit port. The port has four I/O addresses of 8-bits each for the 32 bits. Either Z80 can transmit data to the port; presence of data at the port generates an interrupt to the receiving Z80, and the data is fetched at the next available opportunity.

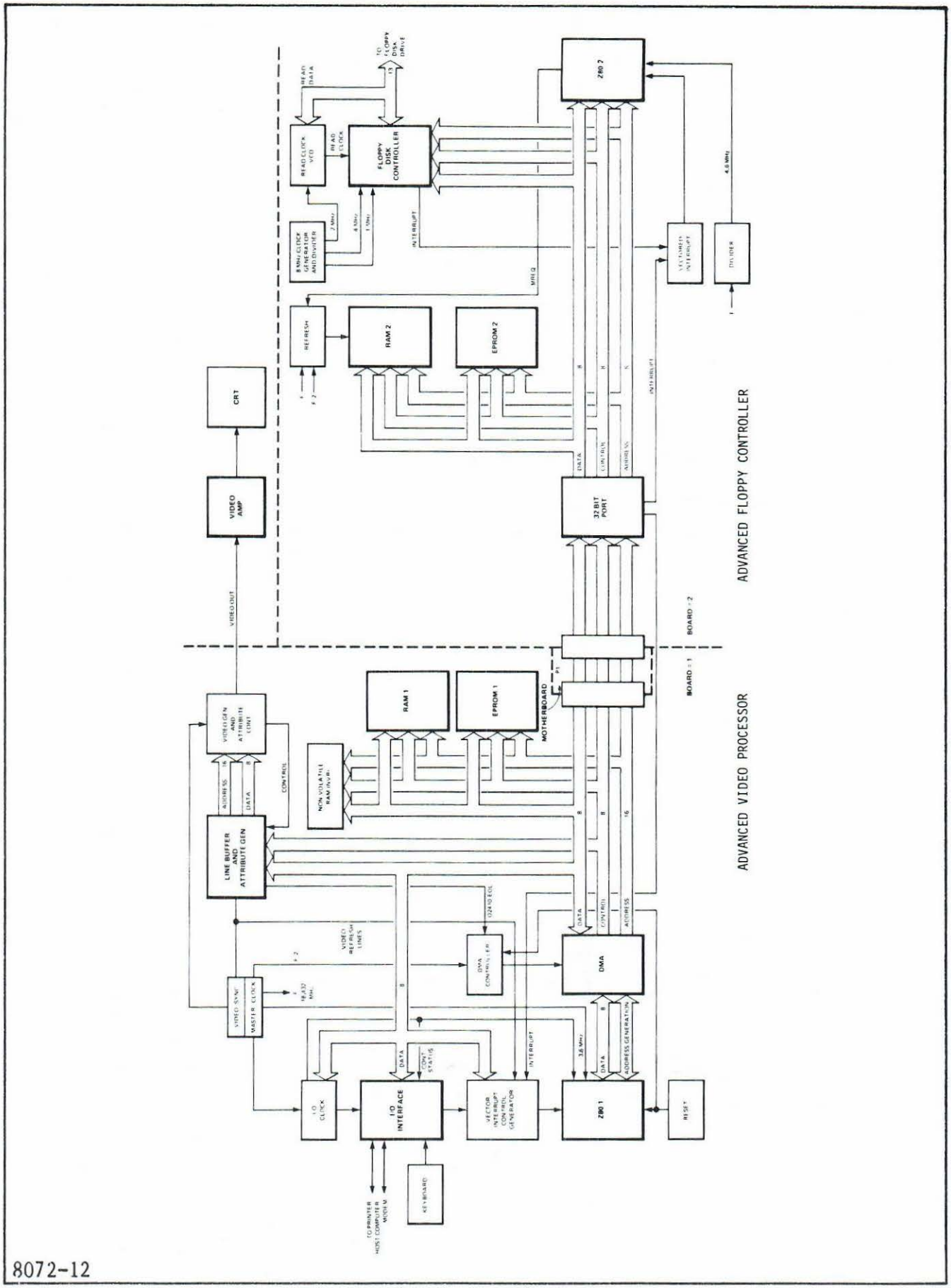


Figure 3-5. System Block Diagram

3.3.2 Vectored Interrupt System

The fully prioritized vectored interrupt system is based on the Z80A Mode 2 Solution, which is programmed at power up. No additional interrupt circuits are required; all interrupt functions take place within the CTC.

Interrupts to Z80-1 are used to fetch data from the two serial I/O ports, and to detect keystrokes at the keyboard. Other interrupts are for the refresh (Line 25) and from the 32-bit port to indicate a data byte waiting to be fetched.

Z80-2 interrupts indicate that data is waiting to be fetched from the 32-bit port.

3.4 SYSTEM DESCRIPTION FOR THE OFFICE DISPLAY TERMINAL (ODT)

The ODT system is shown in figure 3-5, the System Block Diagram. This figure shows the relationship of the circuit functions and the circuit board assemblies. The ODT Terminal has an Advanced Video Processor (AVP) assembly and video display. The S/10 has the AVP and display, but has the additional Advanced Floppy Controller (AFC) for the disk drives and the application programs.

The AVP assembly contains those circuits that are related to the terminal function, such as the input and output ports, the DMA and video processing, master clock and Z80-1, and the microprocessor controller. RAM-1 and EPROM-1, together with the Non-Volatile RAM (NVR) are mounted on this board. The EPROM loads the operating system into RAM-1, and where necessary the terminal personality, which allows it to interface with a host computer.

The AFC assembly carries Z80-2, RAM-2 and EPROM-2, which control the floppy disk controller for the two disk drives. The controller, Z80-2 and RAM-2 communicate with the rest of the system through a 32-bit 2-way port.

3.4.1 Serial Input and Output Ports

All units have three serial ports; two can serve a printer, a host computer or modem, the third is an input port dedicated to the keyboard. Each of these ports is served by a USART to convert the parallel data to serial format for transmission, or serial to parallel for received data. These ports are controlled by a baud rate generator which provides any baud rate from the range specified. Incoming data generates an interrupt to Z80-1. Control and status information is transmitted directly between the I/O ports and Z80-1.

3.4.2 Z80-1, the DMA and the DMA Controller

Z80-1 runs at 4.6 Megahertz, determined by the Master Clock. Z80-1 is dedicated to controlling the I/O Ports, formatting data for the video display, and transmitting video data to the display via the DMA. Z80-1 has direct access to all major parts of the system, except the video monitor which is serviced by the DMA, Z80-2, RAM-2 and the disk controller, which it accesses through the 32-bit I/O Port. Interrupts from the serial, keyboard and 32-bit ports are received and prioritized by a CTC.

Z80-1 supplies the initial 16-bit address to the DMA as sixteen bits of I/O port data (in two 8-bit bytes). Once loaded, the DMA generates the addresses required to transfer data to the Line Buffer under the control of the DMA Controller. The DMA devices transfer data into the Line Buffer until a new starting address is required.

The DMA is controlled by the DMA Controller, which is driven by its own microprocessor and microprogram, allowing it to operate independently of Z80-1. It has its own set of status inputs which allows it to provide data and respond to end of line and data required conditions. Data for the display is stored in RAM-1 in random locations. The DMA takes data for the display and loads it into the Line Buffer in the correct sequence for the display.

3.4.3 Line Buffer and Attribute Generator

Data is stored in the Line Buffer, then supplied to the Attribute Generator, where the display characteristics ar determined, such as font style, video intensity, bold, blink, underline, double high and double wide characters, blanking, reverse video and character mode (80 or 132 characters per line). This data is passed to the Video Generator and Attribute Control.

3.4.4 Video Generator and Attribute Control

This circuit has the Attribute Translator, Cursor Address, and the Character Decode RAM. Blanking, blinking, and video intensity are decoded, and the Video Out signal to the Video Amplifier is generated and transmitted to the Video Electronics, which is part of the display monitor.

3.4.5 RAM-1, EPROM-1, and the Non-Volatile RAM

Z80-1 has a dedicated Random Access Memory RAM-1 which stores data for the functions performed by Z80-1 and the DMA. An additional Non-Volatile RAM (NVR) is supplied for data which can be changed, but unlike the RAM, the NVR retains its contents when power is turned off.

On the System S/10 only, EPROM-1 stores a program necessary to bring the system up when power is first applied. Since RAM-1 has a capacity of 64K, EPROM-1 cannot be addressed independently of RAM-1, so the contents of EPROM-1 are loaded into RAM-1 for execution. EPROM-1 may also contain the personality required for communicating with a host computer. Either of the units may have personalities stored in the EPROM.

3.5 SYSTEM DESCRIPTION FOR SYSTEM S/10

The system S/10 description for the terminal part of the S/10 is identical to the description given in 3.4. The unit has the addition of the AFC board described here.

3.5.1 Z80-2 and the Floppy Disk Controller

Z80-2 controls the operation of the floppy disk controller and its interface with the 32-bit port to the DMA. Z80-2 runs from a 4.6MHz clock. This part of the system operates independently from the rest of the system, exchanging data through the 32-bit port, with the exception of a reset signal from Z80-1.

The floppy disk controller is a single chip which interfaces the disk drives to the data, address and control buses. All signals received from the drives, including data, pass through the controller; all control and data signals to the drives are generated by the controller. This controller also provides special syncs for reading data, and precompensation during data writes.

RAM-2 has a capacity of 64K, and stores data read from the active floppy disk, which includes the CP/M operating system and the application program in current use. It also stores data being transferred between the disk controller and RAM-1, Z80-1, or the I/O ports. RAM-2 has its own refresh generator, which operates during Z80-2 refresh cycles.

EPROM-2 loads RAM-2 during initialization and reset at the same time as EPROM-1 loads RAM-1.

3.5.2 AFC Timing

'F' (18.432 Megahertz) is supplied to a separate divider in the AFC assembly to derive the 4.6 Megahertz required for Z80-2.

The floppy disk system has an independent 8 Megahertz clock with a divider, which supplies the 4 Megahertz clock for write precompensation, the read clock VCO with a 2 Megahertz clock, and supplies the controller chip with 1 Megahertz clock.

3.6 ADVANCED VIDEO PROCESSOR CIRCUIT DESCRIPTION

The following contains detailed descriptions of the Advanced Video Processor. The schematics for these circuits are contained in Section VIII, Reference Data.

3.6.1 The Z80-1 CPU

The microprocessor (12E, see Schematic Sheet 1-1) is a standard Z80 device with a 16-bit address bus and an 8-bit data bus. It is driven by a 4.6 Megahertz clock from the Master Clock to pin 6. All other standard inputs and outputs, except HALT, are used in this system.

The Address bus (AD0-ADF) of the Z80 is connected directly to the EPROM(s), and to the device decoders at 17F and 18F, giving the processor direct control over these functions. The Address bus also goes to page 5 of the Schematic to MUXs at 20B and 21B, where an 8-bit address bus for RAM-1 is derived from the 16-bit Address bus.

The 8-bit Data bus (DZ0-DZ7) exchanges data between the AVP microprocessor, the serial I/O ports, the Z80A CTC, and P1 to the 32-bit port to enable data exchanges between the AVP and AFC assemblies. Data is decoded at 10E (schematic page 1) for VIC0-2 (eight levels of video intensity control), CURSTY (Cursor Style), DISPAL (Display Logical Attribures, BLFLG (Bell Flag), WHNBLK (Display Black on White), and SYCMD (Synchronous Mode) which selects CTC or transmission clocks (23E) for the DART 24F. DZ0-DZ7 receives the output from the EPROM(s) when they are addressed by Z80-1. This data bus also goes to Page 5 of the Schematic to the DMA, RAM-1, and the NVR.

Z80-1 uses all of the standard control signals except HALT and RFSH. See table 3-1.

Table 3-1. Z80-1 Control Signals

CONTROL SIGNAL	DESCRIPTION
BUSACK*	Bus Acknowledge, is transmitted to the DMA controller to indicate that the CPU bus outputs are in the high impedance state, together with control signals MREQ*, IOREQ*, RD* and WR*. External circuits can now control these lines.
BUSREQ*	REEND* from the DMA controller forces the address, data, MREQ*, IOREQ*, RD* and WR* to high impedance.
INT*	Causes Z80-1 to interrupt a current routine to service a higher priority request for service.
IOREQ*	Enables decoder 18F when the lower half of the address bus has a valid I/O address for an I/O operation.
M1*	Active output when the processor is in the opcode fetch mode. When combined with IOREQ*, it indicates an interrupt acknowledge cycle is in progress.
MREQ*	Indicates that the address bus holds a valid address for a memory read or write. This is applied to memory decoder 17F.

Table 3-1. Z80-1 Control Signals (continued)

CONTROL SIGNAL	DESCRIPTION
RD*	Active when the processor is required to read from a memory or device. Enables memory decoder 17F, or goes to the read input of the other devices.
RESET*	Resets the interrupt enable flip-flop and clears I, R, and PC registers.
WAIT*	Input from an addressed device to indicate that it is not ready to receive data.
WR*	Indicates to the keyboard port that the CPU has data to transmit.

3.6.2 The Interrupt System and Timer

The interrupt scheme is controlled and prioritized by the Z80A Mode 2 (21F Sheet 1 of the schematic), which does not require any external circuits. The Z80 arrangement provides a daisy chain fully vectored interrupt structure. IE1 is held high, which gives the CTC priority 1, and the other system interrupts feed in via IE0. The IE0-IE1 connections from the daisy chain from the 32-bit port counter 54 to the DART then the CTC. A signal from any of these devices sends an interrupt to Z80-1.

The CTC also supplies timing signals ZCTC0-2 to MUX 23E for the synchronous mode of I/O operation.

3.6.3 The I/O Ports

There are three I/O ports (Schematic Sheet 1). J5 and J6 are RS-232 serial ports which interface via the Z80-1 DART 24F; the keyboard input is via an 8251A USART at 19F.

The DART provides two independent full duplex channels with separate modem controls. The device is programmed at power up for the required system configureation. Parallel data from the data bus is converted to serial format for the output, and serial data from the communications link is converted to parallel format for the data bus. The signal inputs and outputs are listed in table 3-2.

Table 3-2. I/O Port Input/Output Signals

I/O SIGNAL	DESCRIPTION
B/A*	Selects the A or B channel. B is selected when ADZ0 is high.
C/D*	Selects whether control or signal data is transferred between the processor and the DART. Selects control data when AD1 is high.
CE*	Chip enable, selected low from decoder 18F output ESI0*.
CLK	Input Φ from the Master Clock.
CTS*	Clear to send, enables A or B transmitter.
DCD*	Data carrier detect, enables the A or B receiver.
IEI	Interrupt enable in, to a higher priority device.
IEO	Interrupt enable out, to a lower priority device.
INT*	To Z80-1, to request an interrupt.
M1*	Machine cycle one from Z80-1, operates with RD* and IOREQ*.
IOREQ*	Input/output request, used in conjunction with B/A, C/D, CE*, and RD* to transfer commands and data to and from Z80-1.
RxC*	Receiver clock, selected from MUX 23E. When SYCMD from decoder 10E is high, 23E is in the synchronous mode. When SYCMD is low and the B inputs are selected, 23E is in the asynchronous mode.
RD*	Active when a memory or I/O read is in progress.
RxD	Receive data from A or B channels.
RESET*	Disables receivers, transmitters, and interrupts.
RTS*	Request to send.
TxC	Transmitter clock for A or B, see RxC above.
TxD	Transmit data to the A or B channel.

3.6.4 Device Enable Signals

There are two decoders on Sheet 1 of the Schematic which enable the I/O devices and memories.

18F is a 1-of-8 decoder with ADZ2-ADZ4 as an input, and enabled by ADZ5-ADZ7, IOREQ*, and MIZ*. This selects the CTC; DART; Keyboard Port; octal flip-flop 10E; DMA control; enable NVR; Blink Control Register 21E respectively.

The BLINK ON and CURSOR ON signals are derived directly from DZ0 and DZ1 via 21F, when it is strobed by ECUR*. The Q5 output from 21F goes to ROM 17F through a jumper (installed in the S/10 only). This is part of the address applied to the ROM, which selects the EROM required, EROM0-EROM3, DMA control (29B); RAM-1 (RD*); RAM output buffer 21D enable (ERD0); or RESWT* which puts Z80-1 into the Wait state.

3.6.5 Master Clock and Divider Chain

The Mater Clock is generated by 18.432 Megahertz Oscillator Y1 (see Schematic Sheet 2). The output is the fundamental system frequency, designated 'f', and is distributed to 6C pin 1, to clock the DTRCK and DTRCK* (Dot Rate Clock) signals at the f frequency; note that the DBLWB (Double-Wide) signal to 3C-11 haves the frequency of the DTRCK signal for double-wide characters. f is distributed to other circuits where this frequency is required.

f is applied to 3C pin 13, which divides the frequency by 2, giving f/2 of 921.5 kilohertz. f/2 also drives the divider chain 1E, 1D, 3D, 1C, 2D, and clocks out the vertical blanking pulse VB and VB* from 3C pin 5. f/2 is distributed to other circuits in the system.

The divider chain comprises five LS163 counters formed into a multistage counting scheme. The first counter outputs Φ , the basic Z80-1 clock. The Q1 output from 1E, half of Φ , is the clock for the keyboard port 19F.

The video sync clocks are derived from the divider chain as follows:

1. HORIZ and HORIZ* from 3D-12.
2. 9.4KHz from 3D-11 to the keyboard port for the USART read clock.
3. Speaker drive from 1C13, a square wave at 2.2KHz, used in conjunction with BLFLG for alarms and KEYCLICK for the key press audio response.
4. An additional counter 2C generates the VERT* to the CRT, and VB and VB*, vertical blanking for the Video Out signal.
5. Counter 4E generates the Line Buffer timing for the normal display and for the status line, Line 25.

3.6.6 Line Buffer Control

Line Buffer control is achieved by counter 16A, ROM 15A, and Register 13A (see Schematic Sheet 3). The counter is loaded when 16A-11 and 13A-19 are both high. The counter counts up, clocked by F to 13A latch. It is set up to loop at count 8 and 9 until data is transferred by DMA into input register 19B. At that time, 16A is allowed to count 8, 9, A, B, 8, to generate a WRite pulse. WED, to transfer the data into line buffer RAM, 12B and 13B. The next character is loaded when 19A is reset by LDCRS*. This ROM output is latched by 13A and outputs the load commands required for the complete operation, including:

1. 13A-15 clears the Read Counters, and Line Buffer Control Counter.
2. SCCE, SCroll Counter Enable.
3. LDCRS, Load Cursor.
4. LDE, Load Enable (allows Line Buffer Counter to advance).
5. LAB*, Load Input Counters (exchanges Read and Write Counters).
6. E, Read Counter Enable.
7. WE, Write Enable for the Line Buffer RAM.

3.6.7 Line Buffer

Data for the Line Buffer is received from RAM-1 over bus D0-D7, and stored in the Data Input Register 19B (see Schematic Sheet 3). D4-D7 goes to ROM 16B, End of Line and Logical Decode, which provides End of Line for the DMA Test Decoder, 27B on schematic sheet 5. Data is held in this buffer for one clock, then output as R0-R7, and loaded into the Line Buffer RAMs 12B and 13B by WED. Data to the Dual 1-of-4 decoder 5B causes data to be loaded into the counters and registers in the Line Buffer.

Data R0-R7 is output from RAMs 12B and 13B, and sent to the Line Buffer. The Line Buffer is a series of counters and registers 9B, 8B, 7B, 3B, 4B, and 14B, see Schematic Sheet 3.

9B is a counter loaded with the display character during byte 1 (refer to 3.2.4 for details) from Data Bus R0-R3. It is loaded by SCCE*, and held by VB* during the video blanking interval. A terminal count output generates TBR and CHLD, which loads each character.

Counters 7B and 8B are the Font Registers, and are loaded with byte 2 by LDFNT and INDTCK. 8B loads the font, and 7B is the character generator control. Outputs ENCH (Character Enable) and L0-L4 control the character outputs on sheet 4. When R0 and a coded byte are loaded into 7B, each raster repeats once, and a double high character is generated.

Byte 3 is loaded into 3B to generate timing for the video attributes. Each signal is delayed by one clock in 3B, 2B and 1B. DBLWD halves the frequency of the Dot Rate Clock, which doubles the width of each character when active. LDFNT loads the character output counters 13C, UNDLN, RVID to the Attribute Translator 8D, and DT3D to control the Font Select ROM and the Dot Rate Clock.

Byte 4 is loaded into Font Register 4B. This provides the font information FT0-FT3 to the Font Select ROM 11C (sheet 4), Serializer 15B (DT0D), and the Dot Counter 13E.

R0-R7 is applied to latch 14B. This generates CH0-CH6, including the ROM output at 12C, which is the character in ASCII code. This is clocked through 14B by CHF* derived from J-K flip-flop 7A from NCHAR and RSTCHF reset character font. The character is loaded into counters 13C and 14C, and applied to character decode RAMs 16C and 16D. An optional arrangement is to have these two RAMs replaced by a single ROM at 16D. There is a strap (set at the factory) which selects the write enable for either case: when two RAMs are installed, 1-2 and 3-4 are strapped, which selects the write enable for the RAMs, and selects one or the other with chip enable CE*. When one ROM is installed, 2-3 is strapped and only CHWE* is used. The RAM/ROM output CHF0-CH7 is applied to the serializer 15B and the Dot Counter 10C.

3.6.8 Attribute Generator and Cursor Address

Data inputs R0-R7 laod the cursor address into 10B and 11B when LDCRS* is true (see Schematic Sheet 4). CURSON ON from decoder 21E on sheet 1 clears out the cursor counter to produce the blinking cursor. An output is fed back to the Attribute Translator, 8D. This provides inputs to the video on/off, bold video out, and half intensity video output circuits.

VIC0-VIC2 are the video out overall intensity control to the output transistors Q4-Q5, giving eight levels of intensity. Video on and off control is effected via CR9: half intensity through CR8.

3.6.9 Character Generation

The output of the Character Decode RAM goes to 15B, a parallel-in serial-out shift register, active when pin 15 is low and clocked by pin 7 (see Schematic Sheet 4). These conditions are controlled by the Dot Counter 10C, which receives data from the Font Select ROM 11C. CHF0-CHF2 are the font select inputs. The load next character condition occurs when the Dot Counter gets to a carry condition.

3.6.10 Video Out

The character code CHF0-CHF7 is applied to Serializer 15B, either directly (CHF4-CHF7) or via ROM 11C. 15B converts this parallel form into a serial stream at pin 13. This serial output is NORed with the HORIZontal pulse, then passes through register 9E, pins 8 and 9, and is divided into two paths. The path through 9E-2 and 7D-6 is the normal video path. The alternate path via 7C-9 (active when CHF0 is high), is turned on and off one-half pulse earlier by the Load Next Character signal at 3A-3 and 7C-5, producing the half-dot shift to the left.

The signal at 7D-8 is the Video Out signal at the dot rate. The signal is EXORd at 7D-8 with pin 19, the optional graphics input. A second EXOR gate 8E-8 produces reverse video when required. The signal is applied to CR2 and the base of Q5 to be output via pin 11 to the Video Electronics assembly.

The output level at the base of Q5 is blanked by the HORIZ and VB signals via CR1, and modified by VIC0-VIC2 which sets the video intensity to one of eight levels. Bold adds to the voltage at R22 via R19. Half intensity is produced when HALF* is applied to CR3 and R18. The Video Out signal is transmitted to the Video Electronics Assembly via P1-9.

3.6.11 Direct Memory Access (DMA)

The Z80 provides the initial data (D0-D7) and the addresses (A0-A15) required for each DMA operation. The DMA comprises four 2911 microprogram sequencers 20A, 21A, 22A, and 24A. They are 8 bits wide, and derive data from one of three sources, selected by S0-S1:

1. The R inputs from DZ0-DZ7, going directly to the mux;
2. A four word push/pop stack manipulated by PP and FE;
3. The program counter register incremented by Cn.

The tristate outputs (enabled by OE* when 24B-3 is low) are available at RAM-1 as A0-A7.

PP and FE push and pop the stack. These signals, together with the S0-S1 controls are generated by ROM 27A, which in turn is driven by 30A sequencer. On increments the output if it is 1. REM selects the most significant data, 28B-9 output the least. This DMA output goes to the 8-bit address input to RAM-1. The last bit supplies the carry bit to 30A.

3.6.12 The DMA Controller

The DMA controller is made up of a 2911 sequencer 30A, ROM 29A, 27A, 28A, Register 29B, and MUX 30B. At power up or when the system is reset, RESET* resets 6E, a 2911 microcontroller. The output addresses 29A, which contains the microprogram for the controller 30A. This starts up the sequence which sets up the DMA controller to handle data transfers between the Line Buffer and RAM-1. 29A feeds back the function select S0-S1 to 6E.

The 2911 outputs, Y0-Y3, go to ROM 28A. Outputs 01-03 select an input at the Test Decoder 27B. A test condition generates MREQ (memory request) during DMA cycles with Z80CY, MST address control, and 30A control function.

Mux 30B is a test control mux which selects the A0-A4 or B0-B4 inputs depending on the output of 27B, an 8-input inverting mux. The output is set by the input condition being looked at, as follows:

5F INPUT	TEST CONDITION
0	Continue program (tied high to be always true)
1	Bus acknowledge
2	DEOL, delayed End of Line
3	DREQD, data required
4	Load status line (leading indicator)
5	Z80-1 RAM Request
6	CAS, indicates the end of a DMA memory cycle
7	Load Status Line interrupt (trailing indicator)

This selects either test true (high) or test false at mux 30B, which selects output pins 5 and 6 of 28A and 29A pin 9, or two bits from pins 1 and 2 of 28A with the MSB of 29B pin 7 recycled to maintain its status. The output of 30B goes to 29B, and is clocked through with MQ and ZCY by F/2, which ensures that all of these signals are synchronized. MQ becomes MREQ which is a memory request, and ZCY becomes Z80CY which allocates the data bus to Z80-1 when high, and to the DMA when low. These two signals allow the DMA to load the Line Buffer.

3.6.13 Initializing With EPROM-1

The PROM enable sequence starts when RESET* becomes true. When PROM decoder 17F is addressed by ADZD-ADZF, 17F selects EROM0. The EPROM is addressed by ADZ0-ADZF, and the operating system is loaded into RAM-1.

3.6.14 Non-Volatile RAM (NVR)

The Non-Volatile RAM is addressed, loaded and read over the data bus to Z80-1 (see Schematic Sheet 5). Control for the NVR is derived from the following functions. CS2 is tied low.

CS2	CS1	FUNCTION
0	0	Write
0	1	Read

During Read or Write, the cell address is derived from DZ0-DZ7 from the Z80-1 data bus. Data is written in by access to I/O address 03H causing pin 9 of 30D to be selected (low), which clocks data on the bus through 28E; this signal also sets CS1 low via the 30C J-K flip-flop. Decoder 30D is enabled when ENVR* is true.

Power for the NVR is obtained from VCC (+5V) and a -29V supply from the DC to DC converter made up of Q7, L1, CR8 and R41-43, driven by 1.8 Megahertz.

3.6.15 RAM-1

RAM-1 is located at 22D-28D on Schematic Sheet 5. The RAM address is selected from ADZ0-ADZF by MUXs 20B and 21B by S from ROM 28A. When S is low, 1A-4A inputs are passed to the outputs. Data to and from RAM-1 is transmitted via 2-way tristate buffer 21D which is enabled by CAS and ERD0 from sheet 1 enable decoder 17F. CAS (Column Address Strobe) and RAS (Row Address Strobe) for RAM-1 are generated by the ROMs in the DMA Controller.

3.7 ADVANCED FLOPPY CONTROLLER CIRCUIT DESCRIPTION

This section gives a detailed circuit description of the Advanced Floppy Controller assembly. This assembly is installed only in the S/10. Schematics for this assembly are shown in Section VIII, Schematic 051300, sheets 1 through 3.

3.7.1 AFC Timing

The timing for this assembly is derived from the Master Clock frequency 'f' in the AVP. This clock is passed through the connectors J1-20 and delayed one clock as Bf. This clock is passed through 9D on sheet 1 to drive Z80-2, address MUXs 3C, 4C, 5C and 6C, and as ZIO to drive the counters for the 32-bit port.

3.7.2 The Microprocessor Z80-2

CPU Z80-2 (9C on Schematic Sheet 1) controls the operation of the Advanced Floppy Controller (AFC) assembly. Z80-2 data buses are designated DB0-DB7. This bi-directional bus exchanges data between Z80-2, the disk drive controller (17B on sheet 3), the 32-bit port to Z80-1 (12C-15C on Sheet 2), RAM-2 (1E-12E on Sheet 1), and counter CTC (13B on Sheet 2). The EROM output is also passed to this data bus. DB0-DB5, latched at 15B, provide the SIDE* and SEL0-SEL1* signals to the disk drive.

Address bus AB0-ABF addresses the EROM at 7C, RAM-2 via MUX 3C-6C, the CTC for data to Z80-1, as well as decode functions for the controller, and 32-bit port. The microprocessor is reset by the system reset from J1-28 and ZRST.

3.7.3 EPROM-2

The EPROM-2 7C is addressed by AB0-ABA from Z80-2 (see Schematic Sheet 1). During initialization and reset, it is enabled when CE pin 18 goes low momentarily when 10D is set by the ZRST signal. The contents of EPROM-2 are transmitted over DB0-DB7 to RAM-2.

3.7.4 Z80-2 Vectored Interrupts

The interrupt system is contained in the Z80 CTC at 13B. The interrupt priorities are determined internally, so that no external interupt circuits are required. The Z80 CTC at 13D supplies the interrupt to Z80-1 when data is in the 32-bit port awaiting transmission to the AVP.

3.7.5 32-Bit Port

The 32-bit port passes data between the AVP and AFC in both directions. It comprises four register files. 12C and 14C transmit data from the AVP to the AFC: 13C and 15C transmit data from the AFC to the AVP. Each file stores four 4-bit words. Separate read and write addresses allow data to be written in and read out simultaneously. WA and WB determine the write address when GW* is true; RA and RB determine the read address when GA* is true. Note that AB0-AB1 are both the read address lines for incoming data, and the write address line for outgoing data.

Read and write enable signals are generated by 1-of-8 decoder 17C and 16D. AB2-AB4 from Z80-2 are decoded into CTC external clock timer triggers, and into the read and write enables for the disk drive controller. Similar signals from Z80-1 on the A0-A7 bus perform symmetrical functions for data from the AVP assembly.

3.7.6 Floppy Disk Controller

The floppy disk controller 17B (see Schematic Sheet 3) performs all of the functions necessary to read and write data to and from the floppy disks. System data passes between the controller and Z80-2 via the DB0-DB7 data bus. Control comes from Z80-2 via AB0-AB1, which select the internal registers. See the Floppy Disk Formatter/Controller section shown in Reference Data section of this manual for a detailed description.

Inputs to the controller from the disk drive are INDEX* to mark the index hole. TRK0* for track 0 detection, WRPRT* to signal that the disk is write-protected, and RDATA* for data from the disk, which is normally high, going low for 800ns to denote a mark. An external signal is required to determine whether a mark is a clock or data, and this is supplied by the Voltage-Controlled Oscillator 22D. This generates a variable frequency of approximately 1 Megahertz, based on the voltage present at pin 2. The Data Request Line indicates a valid data read NDRQ, which is transmitted to Z80-2 via DB7. Similarly, IRQ indicates termination of a disk operation to Z80-2 via DB0. The VCO output is clocked into the controller through 19C pin 8 and 18A pin 9.

The VCO is able to regenerate the read data clock by comparison of its output frequency with the read data pulses from the disk, being shaped by 20B pin 12 and 20B pin 13, where their phase relative to the VCO is determined at 24B pin 6. This phase differential is filtered and amplified by OP Amp 26N at pin 7 and the surrounding RC components, where it becomes a correction voltage to the VCO at 2 through R19.

16B pin 37 is tied low for double-density recording (DDEN), which utilizes the modified frequency modulation technique, using a self-clocking feature for high density data on the disk. Master Reset, MR, is tied high in this application.

The SIDE*, SEL0*, and SEL1* controls come from register 15B and determine the side of the disk to be used, and whether drive 0 or 1 is to be selected. These signals are clocked by NWREXT from the I/O port decoder on Schematic Sheet 4.

The remaining signals to the floppy disk drive are STEP* and DIREC* which control the head motion, and WGATE* to enable the data write function. These signals come directly from the controller.

Write data comes from 16A, pin 9, which obtains its inputs from 17B pin 31 (WDAT), pin 17 (EARLY) and pin 18 (LATE). When register 15B pin 10 is low, precompensation is enabled. This data steam is clocked at the standard rate. 16A provides write precompensation. The controller determines if the bit to be written should be synchronized with the clock, or written early (pin 17) or late (pin 18) to compensate for the anticipated bit shift from the media.

3.7.7 Disk Controller Clocks

The major circuits on the AFC share the same clock generator, shown around 15A (see Schematic Sheet 3). It is driven by an 8 Megahertz oscillator, whose input is divided down to 1 Megahertz for the controller chip, 2 Megahertz for the VCO, and 4 Megahertz for the write precompensation device 23B.

3.8 THE MOTHERBOARD

The Motherboard is the interconnection for the Power Supply, AVP and AFC boards. The schematic is located in Appendix. Apart from the Speaker and two drive transmitters for the Keyboard Enable KEYBOEN, the Motherboard has only the following connectors:

P1 to the AVP assembly.

P2 to the AFC assembly.

P3 to the Power Supply.

P4 to the Video Electronics assembly.

P5 is for a future development. (Not Used)

P6 is for an optional modem.

P7 is for the Graphics option.

3.9 DISK DRIVE CIRCUIT DESCRIPTION (S/10 Only)

The basic functions of the flexible disk drive are to record and read digital data on a diskette, and to receive and generate the control signals necessary for completion of the read/write functions. All of the electronics of the disk drive are contained on a single printed circuit board assembly (PCBA).

Figure 3-6 is a functional block diagram of the following mechanical and electrical components of the disk drive:

- o Head positioning control
- o Track 00 sector
- o Spindle drive control
- o Index sensor
- o Head load mechanism
- o Side selection
- o Data recording and retrieving
  - a. Write protect sensor
  - b. Write/erase control
  - c. Data recording
  - d. Data reading

3.9.1 Head Positioning Control

The head positioning circuit is comprised of a four-phase stepper motor/pulley/band combination for converting rotational to linear motion. The pulley/band is attached to the head carriage. Signals from the stepper motor control logic drive the stepper motor which, through the pulley/band, move the head carriage assembly. The stepper motor control logic responds to signals from the user supplied interface.

The four-phase stepper motor operates in a "one-phase on" mode. One step of the motor equals a one-track linear motion of the head(s). This one-to-one ratio results in high positioning accuracy and high step rates. When positioned at Track 00 the correct phase on is 4. To move the head(s) toward the center of the diskette, with the DIRECTION line high, the correct phase sequence is as follows:

TRACK	PHASE ON
00	4
01	1
02	2
03	3
04	4

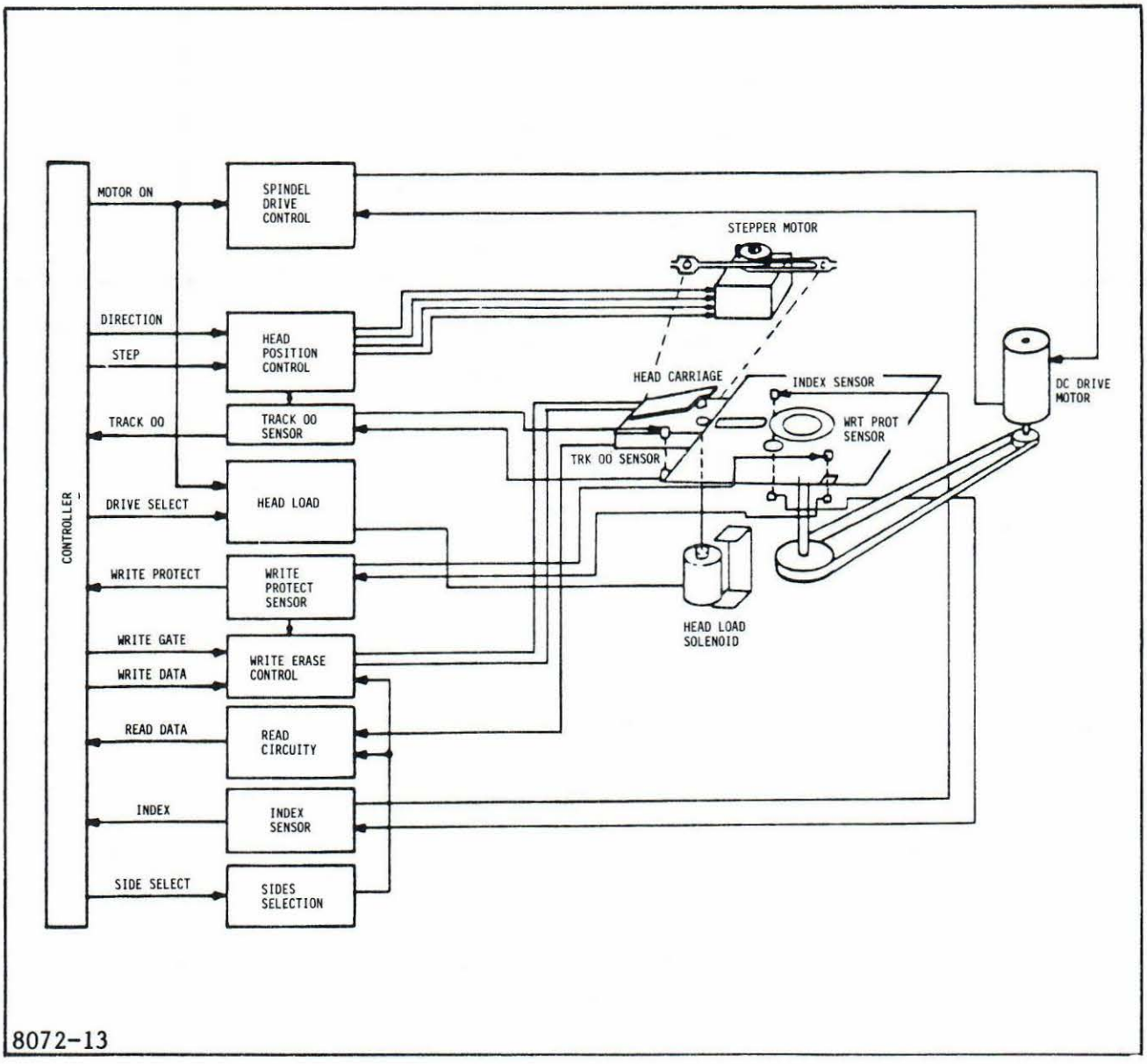


Figure 3-6. Disk Drive Functional Block Diagram

3.9.2 Track 00 Sensor

The track 00 sensor comprises a light source (LED) and a phototransistor positioned on either side of a shutter mounted on the head carriage assembly. The output of this photo detector connects to a conditioning circuit that converts the output of the phototransistor to digital TTL levels. When the head positioning logic positions the head over track 00, the output of the conditioning circuit is a low-true logic level on the TRACK 00 interface line. This signal also inhibits the stepper motor circuitry from responding to any "step out" command.

3.9.3 Spindle Drive Control

The spindle is rotated, via a belt, by a DC motor/AC tachometer combination. The electronics for speed control takes timing information from the tachometer (A), compares it with a reference time (B), and generates a driving voltage for the spindle motor proportional to the difference between (A) and (B). When the MOTOR ON interface line is true the control circuit allows the motor to come up to speed. The control circuit also includes a section that disables the motor drive in case of no tachometer output for approximately 150 milliseconds (possible indication of a binding spindle or motor). The diskette is held on the spindle hub by a clamping mechanism which actuates in conjunction with the front door.

3.9.4 Index Sensor

The LED and phototransistor in the index sensor photo detector are mounted on opposite sides of the index hole in the diskette. The index hole acts as the shutter. When the light beam from the LED passes through the diskette hole and strikes the phototransistor, the output of the phototransistor, through a conditioning cirucit, generates a low true logic level on the INDEX interface line. The position of the phototransistor is adjustable.

3.9.5 Head Load Mechanism

The head load mechanism consists of a head load solenoid and a head load solenoid driver. The interface logic may be connected to energize the solenoid via either DRIVE SELECT or MOTOR ON interface signals. Activating the solenoid causes the diskette to be pressed against a fixed platen and a spring loaded load arm with a felt pad (Model 91) or upper head (Model 92) opposite the head to press the diskette against the head. This load arm is lifted when the front access door is opened regardless of the state of the solenoid.

Head Load Mechanism has been modified on later drives. The solenoid has been removed. The heads are loaded when the access door is closed.

3.9.6 Side Selection

The Model 92 disk drive has two read/write heads; one on each side of the diskette. Therefore, prior to the read or write process the desired "side" (head) of the diskette must be selected. Interface signal SIDE SELECT controls a decoder that enables the read/write amplifiers for either head zero (bottom head) or head one (top head) to be connected into the read/write circutis to the interface.

3.9.7 Data Recording and Retrieving

The drive uses tunnel-erase head(s). The erase gap follows the write/read gap in the head assembly. The erase gap erases the edges of the written track to provide a guard band between tracks to allow for positioning tolerances among drives. The recording and retrieving electronics consist of:

- Write current source
- Steering Circuit
- Erase driver
- Read amplifier
- Differentiator
- Cross-over detector
- Pulse generator

a. Data Recording

To record digital data, current is passed through the winding on the write/read head core which sets up a flux field across the write/read gap. This orients the iron oxide particles on the diskette surface underneath the gap to the same polarity. The direction of the flux field is a function of the polarity of the write current. Data is written by reversing the current through the head. Each flux reversal represents a data bit. The head(s) in the drive uses a center-tapped write/read winding, where the current reversal is accomplished by steering the current through one or the other of the two halves of the winding. Figure 3-7 shows the basic recording technique. The following conditions must be accomplished by the user before the recording can begin:

1. Spindle speed must be stabilized. This condition will exist 0.5 seconds after the MOTOR ON command is issued.

2. Head/media must be stabilized subsequent to the HEAD LOAD command. This requires 35 milliseconds.

3. Head must be settled subsequent to the STEP command. This requires 30 milliseconds (5 milliseconds for motion and 25 milliseconds for settling).

The preceding conditions may be overlapped. It is recommended that the first WRITE DATA command be within 4 to 8 microseconds after WRITE GATE goes true, and the last WRITE DATA command be within 4 to 8 microseconds before WRITE GATE goes false. The erase circuit enables the erase current 430 microseconds after WRITE GATE goes true and disables the erase current 850 microseconds after WRITE GATE goes false. These time relationships are optimized for proper erasure on both inner and outer tracks.

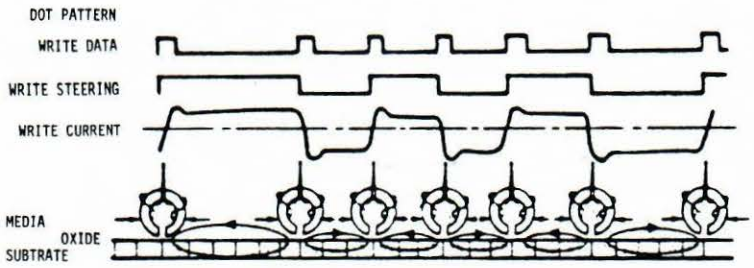


Figure 3-7. Basic Recording Technique

b. Data Retrieving

The retrieving (read) electronics comprises the following elements:

1. Read amplifier
2. Linear filter
3. Differentiator
4. Cross-over detector
5. Digital filter
6. Pulse shaper

Before reading can begin, several conditions must be established by the user system. First, the same conditons applicable to data recording must be met. Additionally, if the previous operation was writing, 1 millisecond must be allowed after termination of WRITE GATE to allow for erase and circuit-settling time. Figure 3-8 shows wave forms in the read sequence. The head generates a wave form is amplified, fed through a low-pass filter, and then differentiated to make the peaks occur at zero cross-over. The read signal is next fed to a cross-over detector, which generates a pulse for each zero cross over. These pulses are fed through a digital filter which removes false pulses. Finally, the pulse shaper generates a one microsecond pulse corresponding to each flux transition. This composite read data is sent to the user interface via the READ DATA line.

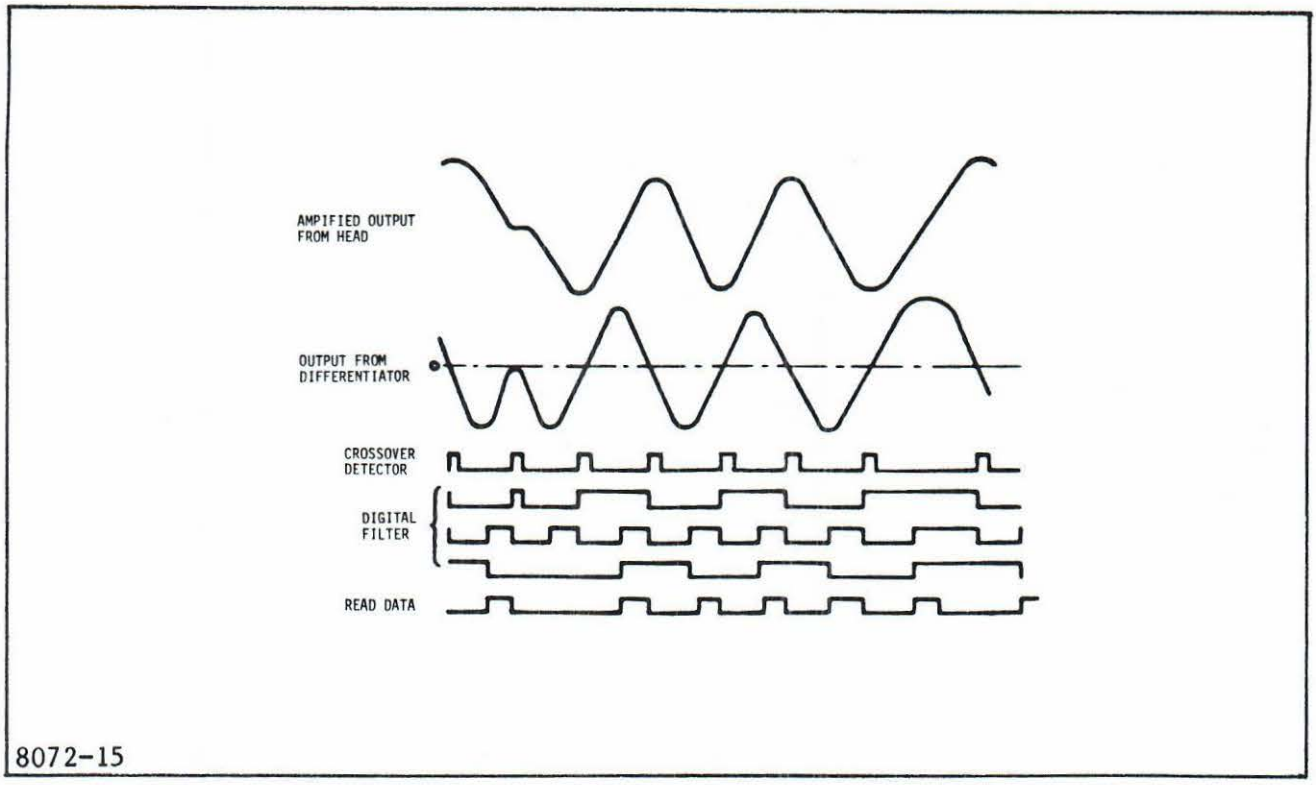


Figure 3-8. Wave Forms in Read Sequence

3.10 VIDEO MONITOR CIRCUIT DESCRIPTION

A block diagram of the video monitor cirucits is shown in figure 3-9. The video monitor incorporates precision CRT's which provide uniformity of display and controlled spot size and geometry. The display is operated from a standard +12 volt D.C. supply.

Input and output connections for the displays are made through a 10 pin edge connector on the main circuit board. Provision has been made for an optional remote brightness control. Schematic reference numbers are pinted on the circuit board to aid in the location and identification of components for servicing.

The monitor consists of a Video Amplifier, a Horizontal Oscillator, a Horizontal Driver, A Horizontal Output stage and three stages of Vertical Deflection (see figure 3-9).

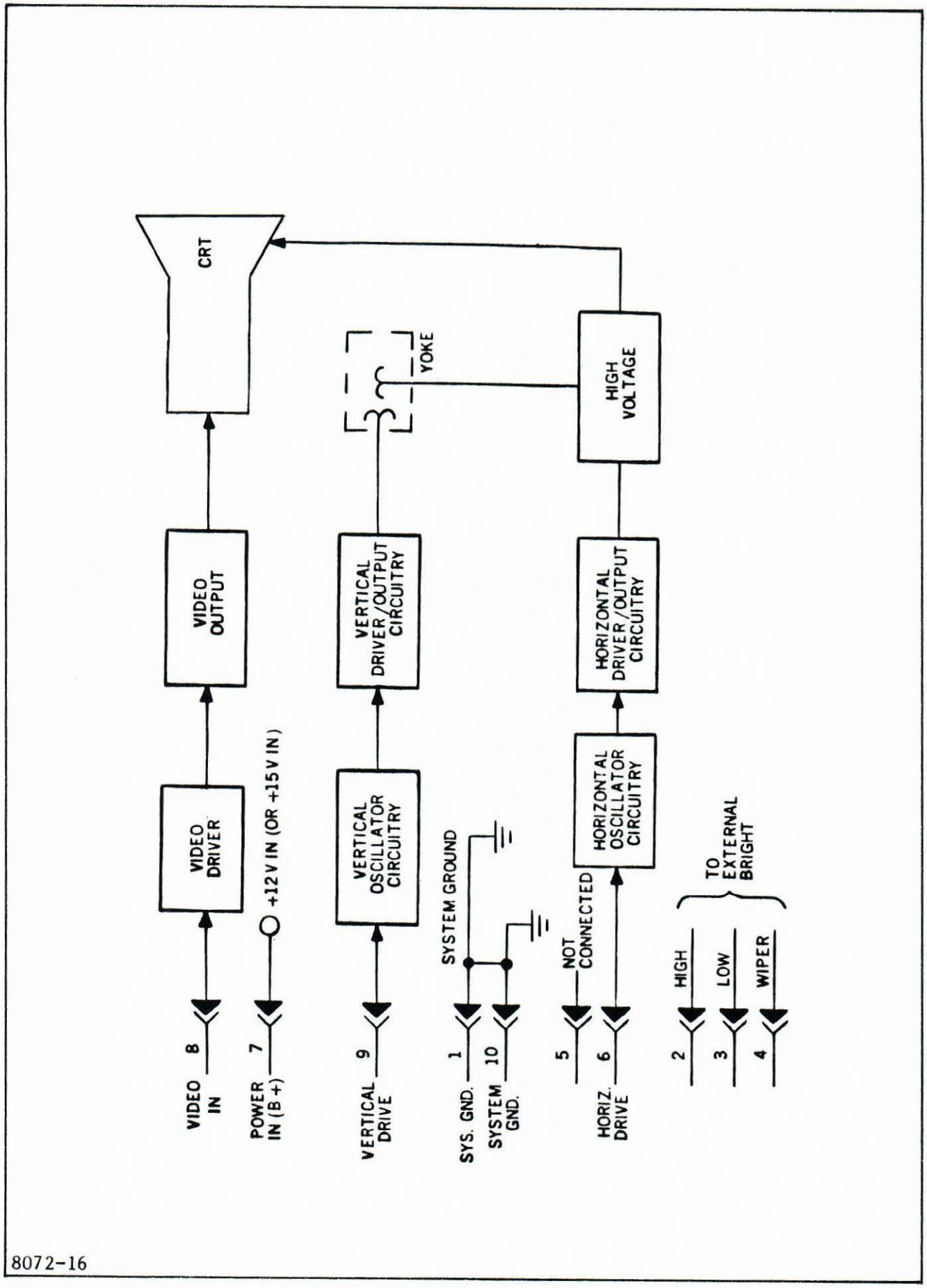


Figure 3-9. Video Amplifier Block Diagram

3.10.1 Video Amplifier

The TTL compatible video signal, input at pin 8 of edge connector, is direct coupled via R402 to the base of the Video Amplifier Q402. Contrast Resistor is used as the load resistor for the video signal source. The RC network (R403, R404 and C401) provides Q401/Q402 with increased gain at high frequencies by altering the collector-emitter load resistance ratio. At low frequencies, C401 appears as an "open" and only R403 is in the circuit. At higher frequencies, C401 "shorts", thereby shunting R403 with R404 lowering the emitter load resistance and increasing the emitter-collector resistance ratio. Therefore, the gain of Q401/Q402 increases. Approximate voltage gain of this stage is 20V.

Resistor R408 provides the collector load for the video output signal. The amplified video is fed forward and direct coupled via R212 to the cathode of the CRT.

3.10.2 Horizontal Driver

The horizontal drive signal, input at pin 6, must be TTL compatible and a series of positive-going pulses of approximately 4-40 usec duration (see figure 3-10). In addition, the leading edge of the pulse may be coincident with the end of the video. The horizontal pulses may be delayed (approximately 1.3 usec) to attain centering of the video within the raster.

At the end of the video period, the horizontal drive signal goes positive and is coupled through C101 to the base of Horizontal Oscillator Q101. This action pulls the base of the Horizontal Output stage (Q104 low, forcing it into "cut-off". Approximately 27 usec later, the negative-going trailing edge of the horizontal drive pulse switches Q103 off, which then allows Q102 to conduct. Base current is now provided to Q104 via the network switching pulse transformer. It is used to generate the pulse voltage of the Horizontal Output Transistor Q104.

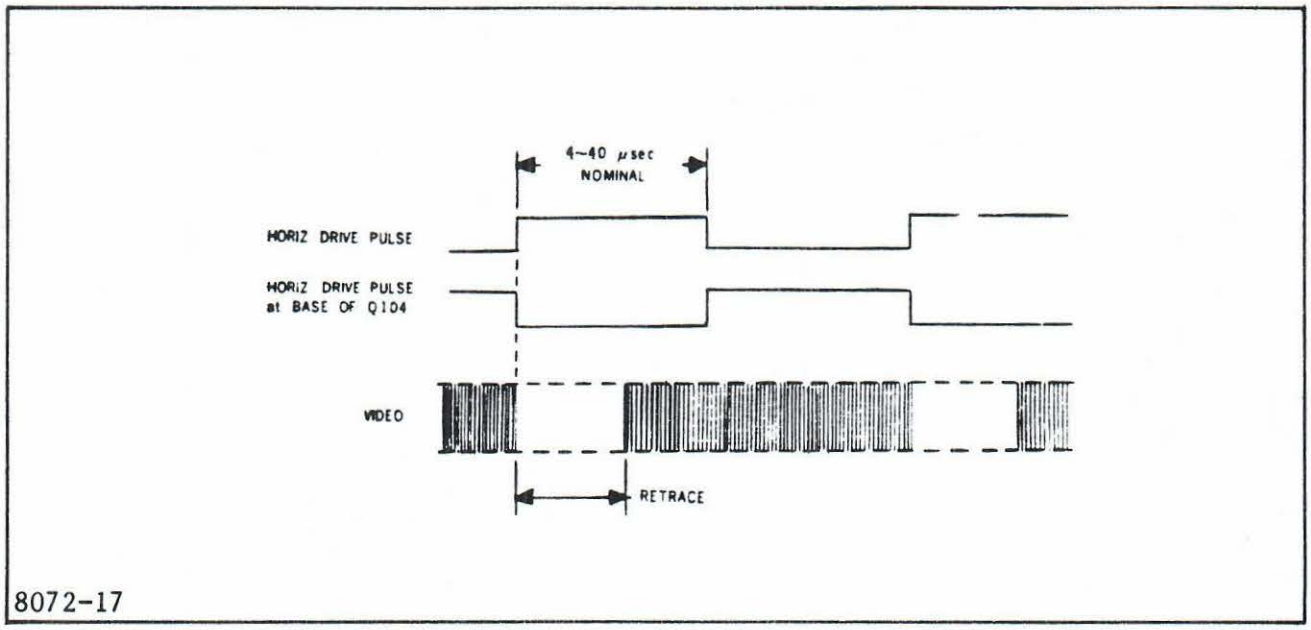


Figure 3-10. Horizontal Drive Signal

At the end of the video period (horizontal drive going positive), the drive pulse at the base of Q104 goes low, forcing Q104 to cut off. This produces a retrace pulse occurring at the end of each line or sweep period that quickly drives the electron beam from the right to the left side of the screen.

Coincident with the retrace pulse, is the dissipation of the yoke current as determined by the LR time constant of the yoke, the primary windings of T1 and the action of D103. When the electron beam travels to about the center of the screen, Q104 turns on to form a current path from the +12V supply through the yoke (L103). The Horizontal Size (L102), and the Horizontal Linearity (L101) coils, to complete the raster line.

The retrace tuning capacitor, C109/C110 forms a tuned circuit with the inductive components of the yoke, L103. The linearity coil, L101, provides optimum horizontal linearity by shaping the deflection current per the amount of magnetic biasing as determined by the position of its core.

3.10.3 Horizontal Output Transformer

Transformer T103 produces secondary voltages via the auto transformer action of the primary winding. The transformer produces +50V, -60V, +600V and +13kV. The +50V supply is used as B+ for transistor Q401. The +600V and the -60V are applied across the brightness pot, R207. In addition, these voltages provide enough range to allow the blanking pulses to turn off the CRT beam during retrace.

The +600V source supplies the second grid, G2, of the CRT, in addition to the variable focus bleeder resistor. The +13kV supplies the second anode of the CRT with B+.

3.10.4 Vertical Deflection

The vertical drive signal, a negative-going short duration spike, is supplied to the unit via pin 9 of edge connector. This drive signal is direct coupled to the base of Q301 via R301, C301 and R303. When the vertical drive signal is false or high, Q301 is cut off allowing C309 to charge toward +12V.

This charging action generates a linear positive-going ramp (sawtooth waveform) applied to the base of Q304, the Vertical Driver stage. When the vertical drive signal goes true or negative, Q301 conducts, discharging Q309 to nearly zero volts. This action forms the retrace portion of the sawtooth waveform. Q304, an emitter follower configuration, transforms the high impedance of the sawtooth waveform into a low impedance drive for Q305, the vertical driver stage.

The sawtooth voltage of the vertical driver Q305 is fed directly to the bars of Q306 and 307. The vertical output transistors, Q306 and Q307 are wired in the standard push-pull configuration. Transistor Q308 doubles B+ during retrace, maintaining less than 800 usec of retrace time.

3.11 THE POWER SUPPLIES

There are two Power Supplies; one is for the ODT Terminal, and a more powerful version for the S/10. The boards are similar in physical size and appearance, and use the same circuit board. The S/10 supply has additional components installed.

Schematics for the Power Supplies are included in Section VIII, Reference Data. The +5V DC level is adjusted by R114 on both boards. None of the other levels have individual adjustments; if they are out of tolerance, the regulator must be replaced.

SECTION IV

MAINTENACE

4.1 INTRODUCTION

This section gives instructions for conducting routine preventive maintenance to both the Office Display Terminal (ODT) and the System (S/10). It contains procedures for troubleshooting to the field replaceable unit (FRU) and for replacing defective components. Adjustment and alignment procedures are also included.

Some of these procedures apply to both the ODT and the System S/10. Where a procedure applies only to the System S/10, this is clearly shown in the text. At the present time there are 3 types of hardware in the field. They can be identified by serial number on the MAI-Basic Four label attached to the back cover as follows:

Phase 1A Hardware (also called Original Phase)

S/10 Phase 1A, Model 4105, Serial Numbers XX 0001 to XX 9999
ODT Phase 1A, Model 4308, Serial Numbers XX 0001 to XX 9999
Note: XX represents 2 alphabetical characters that changed monthly.

Phase 1B Hardware (also called New Style Phase)

S/10 Phase 1B, Model 4105, Serial Numbers CE 401000 to CE 499999
ODT Phase 1B, Model 4308, Serial Numbers VJ 101000 to VJ 999999

Phase 2A Hardware

S/10 Phase 2A, Model 4105, Serial Numbers CE 500000 to CE 599999
ODT Phase 2A, Model 4308, Serial Numbers VL 100000 to VL 999999

Each type of hardware uses a different version of the BB/M or CP/M Operating system software:

Phase 1A hardware uses: BB/M 9.0 or BB/M 9.1
Phase 1B hardware uses: BB/M 9.0B or BB/M 9.1B or BB/M 9.2A
Phase 2A hardware uses: BB/M 9.2B

Operating System diskettes for Phase 1A and Phase 1B Hardware are not interchangeable, the use of an incorrect version of BB/M or CP/M will result in Operating System load failure.

4.2 TOOLS AND TEST EQUIPMENT

Only standard tools and test equipment are required for servicing and repair.

4.3 PERIODIC AND PREVENTIVE MAINTENANCE

Periodic maintenance consists of cleaning the exterior, and a visual check of the unit for signs of damage or excessive wear. The power supply voltages are checked and adjusted if necessary, and the CRT is realigned. Diskette drive units also require regular cleaning and alignment.

Periodic maintenance should be performed as indicated in this schedule:

CHECK	FREQUENCY	ACTION
Cleanliness	Monthly	Clean the case and tube face
Visual Check	As Required	Inspect cables, connectors, etc
CRT/Display	Yearly	Check/align
Voltages	Yearly	Check/adjust
Disk Drives (System S/10 Only)	As Required	Clean Heads

4.3.1 Cleaning

To clean the unit, proceed as follows:

CAUTION

Do not use solvent-based cleaners or abrasive cleansers to clean the cabinet.

1. Turn off power and disconnect the power cord.
2. Using soap and warm water or a mild commercial cleaner, wipe the cabinet exterior with a damp sponge or soft rag.
3. Using an ammonia-based glass cleaner and a soft rag or paper towels, clean the face of the CRT.
4. Using a non-metallic, flat blade instrument (such as a plastic letter opener), lift the keyboard cover. Remove dust from the inside of the keyboard assembly with a soft bristle brush or similar tool.
5. If coffee or a soft drink has been spilled on the keyboard, clean the keyboard assembly interior with isopropyl alcohol.

4.3.2 Visual Check

To check for cabinet damage and wear, proceed as follows:

1. Turn off power and disconnect the power cord.
2. Inspect the keyboard assembly exterior for loose rubber strips (on bottom of assembly), bent or broken hinges, lifted label strips on the keyboard panel, and damage to the assembly finish. If necessary, re-cement the rubber strips using Loctite 416 or a similar adhesive (use sparingly!). If necessary, re-cement the keyboard label strips using Loctite 416 or an equivalent (agins, use sparingly!). Replace the hinges if necessary.

3. Inspect the keyboard connecting cable for broken connectors. Replace the cable or connectors if necessary.

4. Remove the keyboard assembly cover and inspect the assembly interior for loose keyboard mounting screws, stressed or broken connecting wires, and loose or broken keys.

5. Inspect the CRT panel for lifted trim strips. Re-cement them as necessary, using Loctite 416 or an equivalent (use sparingly!).

6. Inspect the rear of the cabinet for loose or missing screws in the power cord and keyboard cable connectors (see figure 4-1). Tighten or replace them if necessary.

7. Open the cabinet cover and inspect the latch for bent or broken hardware (see figure 4-2). Straighten or replace the latch if necessary.

8. Unplug the host (and printer, if used) interface cable from the rear of the cabinet.

9. Inspect the wiring harness for broken or stressed wires. Pay particular attention to the edge connectors on the two boards, the power supply, and the video assembly. Repair or replace the wiring if necessary.

10. Check that connectors on the video circuit card assembly are properly plugged in. Reseat the connectors as necessary.

WARNING

Dangerous potentials may exist when power is off because of charges retained by the CRT anode. To avoid injury, always remove power and discharge the CRT circuits to ground before touching them.

11. Inspect the CRT anode lead for cracks or breaks in its insulation or burn marks, which indicate areas of high voltage shorts caused by the insulation breaking down. Replace the flyback transformer if necessary.

12. Check all wiring for signs of abrasion, cracks, burn marks (such as from a soldering pencil), and any other signs of damage.

13. Repair or replace any damaged wiring.

14. Reconnect the power cord, and other cables.

15. Restore the unit to service.

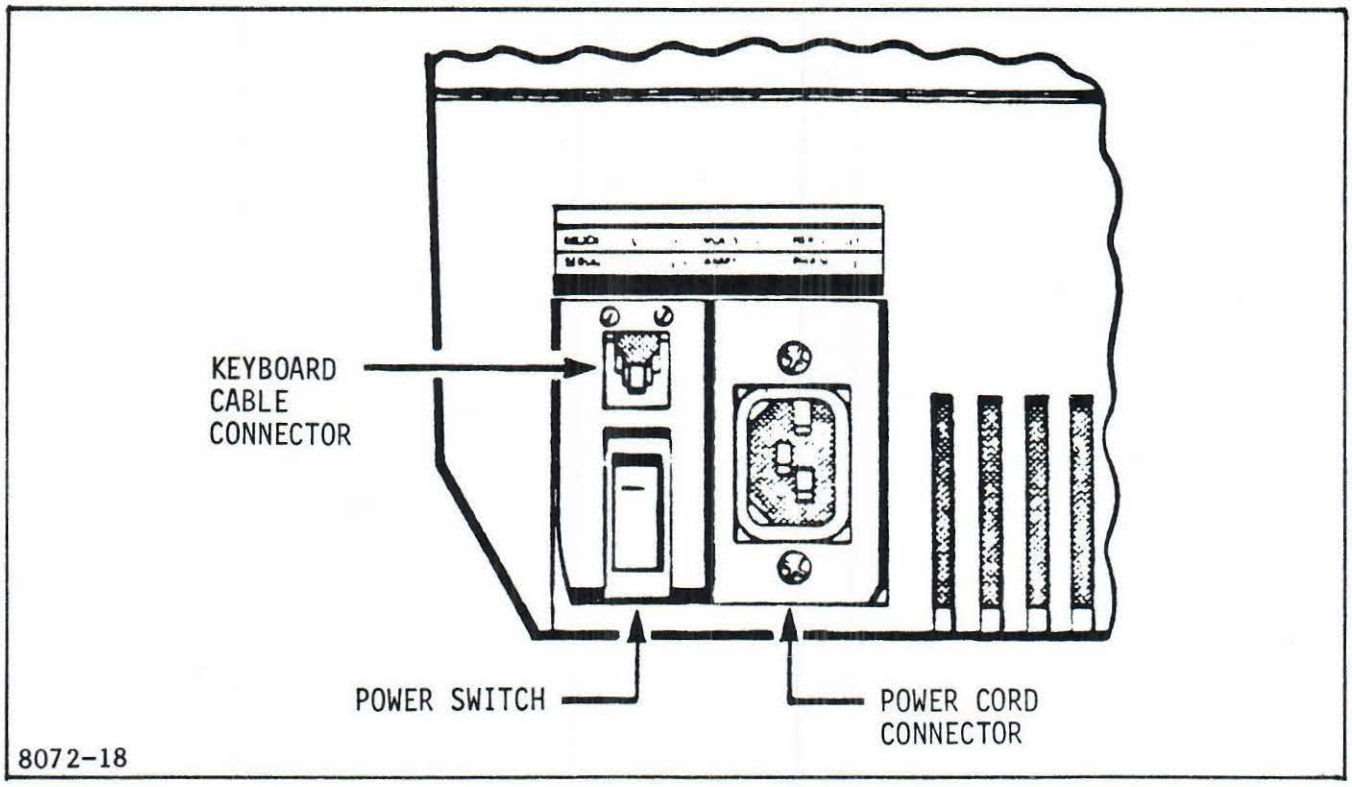


Figure 4-1. Cabinet Rear Lower Left Corner

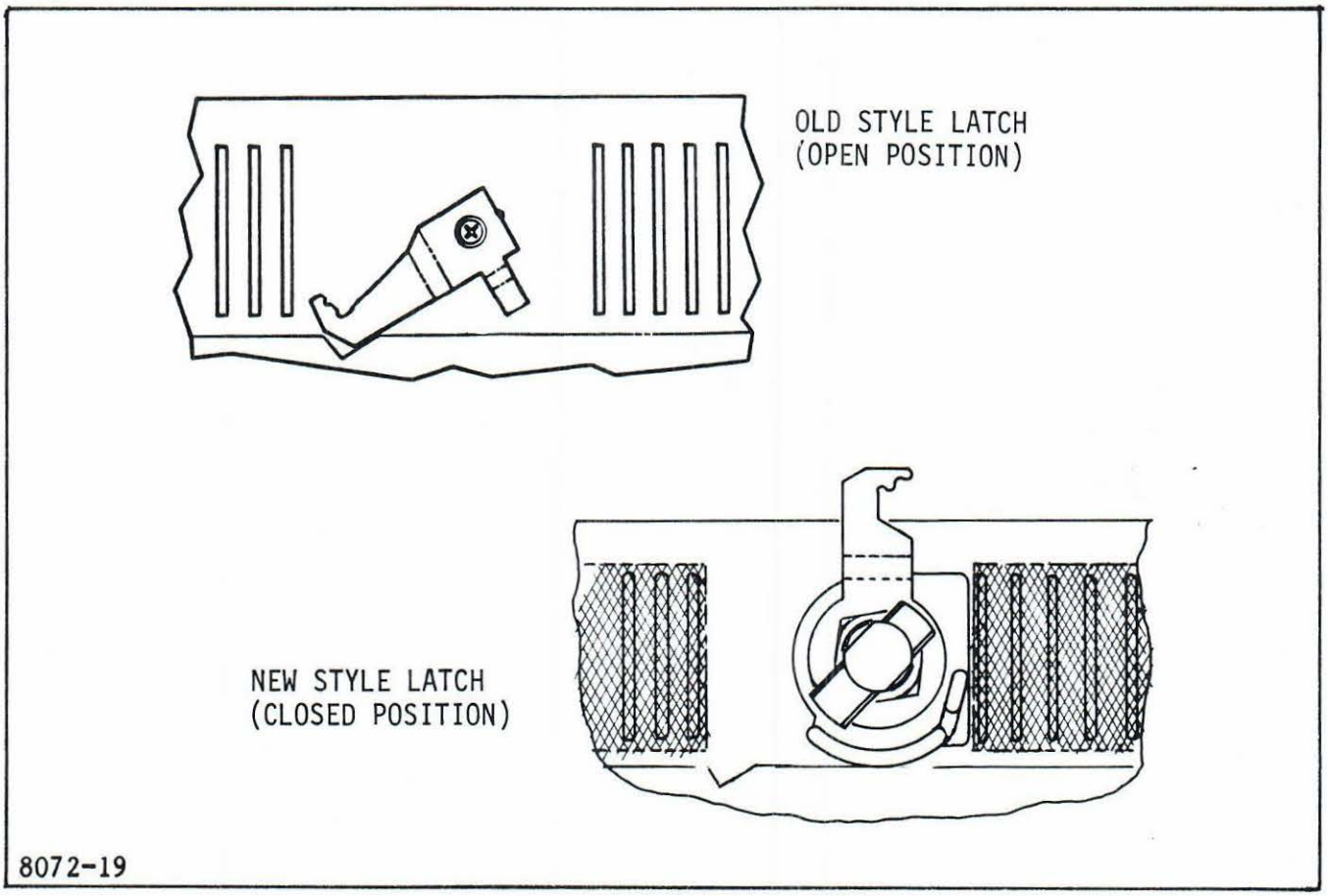


Figure 4-2. Cabinet Cover Latch (inside view, cover opened)

4.4 VOLTAGE CHECKS

The unit has one power level adjustment for +5 volts DC. All other voltages are dependent on the +5 volt supply but they should be checked as part of the adjustment procedure. Out-of-tolerance voltages may indicate either a faulty power supply regulator or a high resistance short in a circuit supplied by the voltage in question. To adjust the +5 volt supply, proceed as follows:

WARNING

Hazardous voltages are exposed in the cabinet at the CRT anode lead and on the video monitor board. Be extremely careful when servicing either the power supply or any area where power terminals are exposed.

1. Open the cabinet, power up the terminal, and set it to Local (press FUNCTION and LINE/LOCAL at the same time to cause Local to appear in Status Line One).

2. Using a DVM, check for +5 VDC on the top trace of the AVP board. (See figure 4-3). The meter should indicate between +5.0 volts to +5.03 volts DC. There is no minus tolerance on this adjustment.

3. If the +5 VDC level is out of tolerance, adjust the resistor on the Power Supply accessible through the shield.

4. On the S/10 system, also check the +5 VDC on the top traces of the AFC board. This voltage should be identical to the voltage measured in step 2 above.

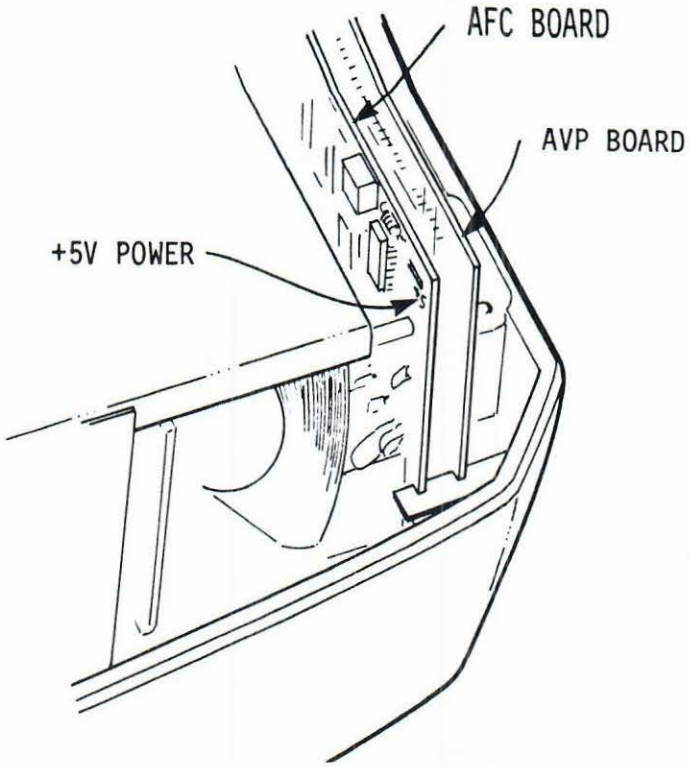
5. Measure the remaining voltages between regulator board connector pins 10, 11, 12, or 13 (Ground) and the following pins:

Voltage	Tolerance	Pin
+12 VDC	±1.00 Volts	5
-12 VDC	±1.00 Volts	4

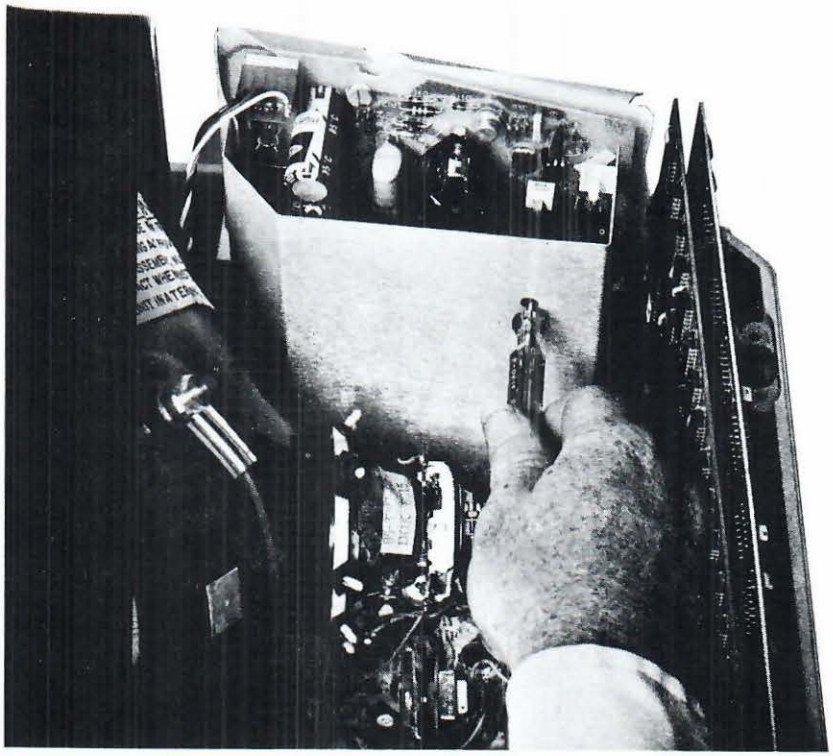
6. If any of the voltages in step 5 are out of tolerance, refer to table 4-1 for troubleshooting information.

4.5 ADJUSTMENT PROCEDURES

After initial installation or after replacement of the Disk Drive Assembly, Video Display Monitor or Video Amplifier, or Advanced Floppy Controller, the following adjustments must be verified and, if necessary, adjusted. The adjustment criteria should also be verified in the event of a malfunction, before engaging in further troubleshooting activity.



+5V TEST POINTS LOCATION



+5V DC ADJUSTMENT LOCATION

8072-20

Figure 4-3. +5VDC Adjustment

4.5.1 DISK DRIVE ADJUSTMENTS (S/10 ONLY)

Listed below are the adjustment procedures contained in this section for the disk drive. The appropriate paragraph should be referred to when performing any of these procedures. It is recommended that a master alignment diskette be kept and that each alignment be verified to the master.

4.5.1.1 Radial-Track Alignment

To perform radial track alignment perform the following steps in the order listed:

1. Apply power to the disk drive. Apply controls to the drive for recalibration to track 00.

2. Insert a CE alignment diskette (DYSAN P/N 802020, MM#529030) and close the door.

3. Sync oscilloscope on leading edge of signal on TP6 (output of 4F-14). Connect oscilloscope probes to TP1 and TP2 (inputs to 2B-1, -14). Set the oscilloscope to 50mV/cm, ac coupled, channel A and B added, with B inverted, 20ms/division. Attach ground probes to TP7.

4. Position the heads to track 32. Load head and apply 32 stepping pulses, with the DIRECTION line low. The carriage should now be located around track 32. The proper phase relationship of stepper motor phases should be: phase 4 = oV, phase 1, 2 and 3 = +12V.

5. With power on, loosen the stepper motor mounting screws on bottom of drive and rotate the motor so that the "cat's eye" pattern appears on the scope and adjacent lobes are within 70% amplitude (see figure 4-4). Tighten mounting screws. Command a return to track 00 and then step back to track 32 to verify proper alignment. Command a seek to track 64 and then step back to track 32 to verify proper alignment.

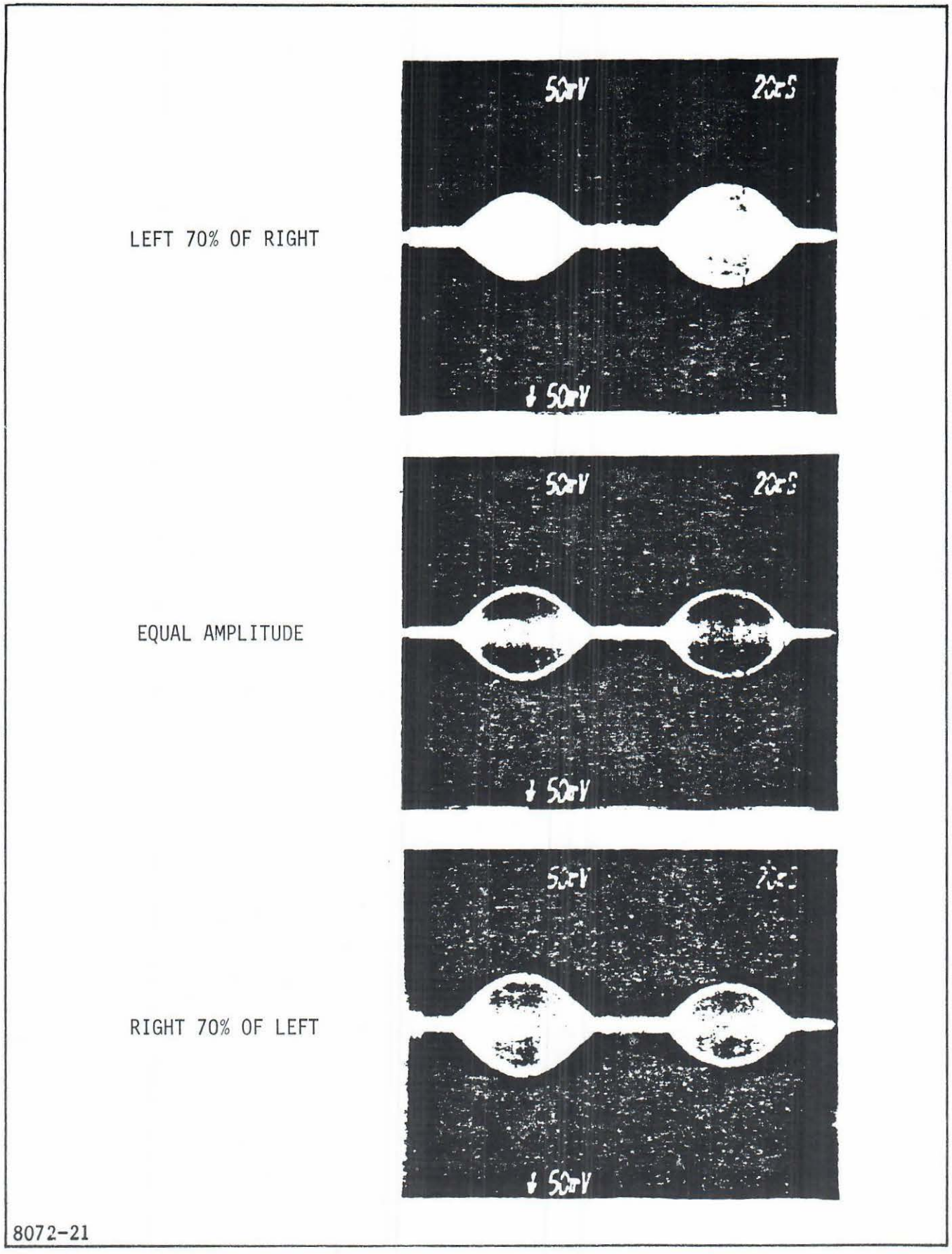
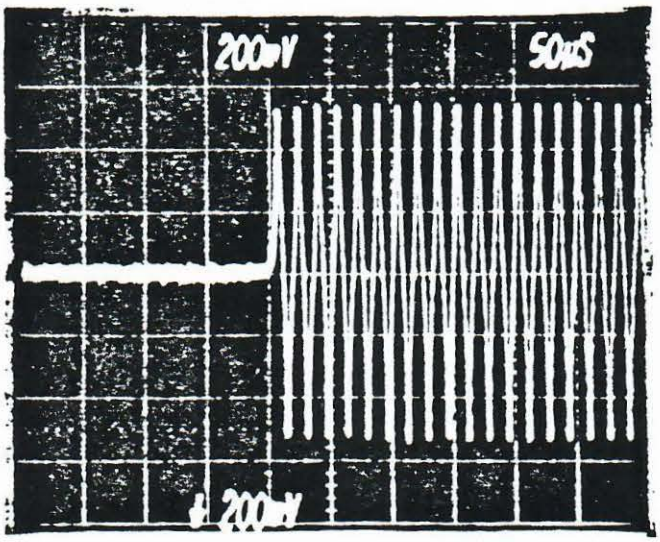


Figure 4-4. Radial Track Alignment Patterns

4.5.1.2 Index-To-Data Alignment

To perform the index-to-data alignment perform the following steps in the order listed:

1. Verify the radial-track alignment. Position the heads to "INDEX TO DATA" track.
2. Set the oscilloscope to 50 microseconds per division.
3. The index sensor mounting screws are located at the bottom of the drive in the recessed area. Loosen the two screws and slide the sensor such that the oscilloscope picture shows a data pattern starting 200 $\pm$75 microseconds from the start of the trace. See figure 4-5.
4. Using a 20 inch-ounce torque screwdriver, tighten the screws carefully so that no variations in the oscilloscope display occur.



8072-22

Figure 4-5. Index-To-Data Alignment Pattern

4.5.1.3 Track 00 Sensor Alignment

To align the track 00 sensor perform the following steps in the order listed.

1. Verify the radial-track alignment.
2. Apply power to the disk drive and select drive.
3. Connect channel A probe to connector J4-12; set oscilloscope trigger to INTERNAL/AUTO.
4. Loosen the two track 00 sensor mounting screws (top/rear of disk drive, adjacent to solenoid) and adjust the sensor for the conditions in steps 5 and 6 following.
5. When the carriage is positioned over track 00 or 01 the signal at J4-12 should be at 0.5 volts (maximum).
6. Command a step-in to track 03. Signal at J4-12 should go to +4.0 volts minimum.
7. Tighten the sensor mounting screws.

4.5.1.4 Speed Control Adjustment

To adjust the speed control perform the following steps in the order listed.

1. Apply power to the disk drive and select drive. Apply 0V to MOTOR ON.
2. Insert a diskette and close the door.
3. Turn disk drive on its side and observe the strobe effect of spindle pulley. If operating from 60 Hz power observe outer trace; if operating from 50 Hz power observe inner trace. Adjust R38 on PCB for a stable strobe pattern. Note that a small amount of strobe "creep" is permissible.

4.5.1.5 Track 00 End Stop Adjustment

To adjust the track 00 end stop perform the following steps in the order listed:

1. Verify the radial track alignment.
2. Verify the track 00 sensor alignment.
3. Apply power to the disk drive and select drive.
4. Command a seek to track 00.

5. Adjust the setscrew located on the left-hand boss in the rear of the drive to approximately 0.010 inch from the end of the carriage (approximately one-third revolution of the setscrew). Command a maximum track seek, then a return to track 00. Assure that the carriage does not hit the end stop.

6. Alternate Adjustment Method: Using an alignment diskette, restore to TRK 00. Assure that a read signal is present. Turn the TRK 00 setscrew clockwise until the read signal amplitude is minimal. Now turn setscrew counterclockwise while pushing back on head carriage until read signal amplitude reaches approximately one-half of its original value. This assures that the head assembly will not restore past TRK 00.

4.5.1.6 Drive Belt Adjustment

The new Model drives all have neoprene (black) drive belts. Older Model drives have mylar (yellow) belts. They are adjusted differently as follows:

1. Mylar (Yellow) Drive Belt Adjustment - Loosen drive motor mounting screws (bottom of chassis). Adjust drive motor so that the tension on one leg of the drive belt is 17 $\pm$1 grams. A tensiometer may be used to make this measurement. Tighten the drive motor mounting screws after adjusting the belt.

2. Neoprene (Black) Drive Belt Adjustment - Loosen drive motor mounting scres (bottom of chassis). Position the drive motor as close to the spindle assembly as possible. Tighten the drive motor mounting screws. No belt tension measurement is necessary.

4.5.1.7 Azimuth Alignment

There are 2 types of Floppy drives in the field, one contains heads with 0 minutes azimuth and the other contains heads with 33 minutes azimuth.

The drives with the 33 minutes heads are identified by a label marked 92S-949, 92S-H049 or 92S-049 attached to the rear of the drive.

All drives without a label or with other numbers are considered to be 0 minutes azimuth.

Head alignment requires the use of the correct type of Alignment diskette:

0 Minutes Alignment Diskette

Sorbus P/N OR997749, Dysan Model 224/2A, Dysan P/N 800180

Index to data (burst)	Track 2
Radial Alignment (cat's eye)	Track 32
Index to data (burst)	Track 68

BFISD 8072

33 Minutes Alignment Diskette

Sorbus P/N MM529030, Dysan Model 206/30, Dysan P/N 802020

Index to data (burst)	Track 8
Radial Alignment (cat's eye)	Track 32
Index to data (burst)	Track 56

CAUTION

Positioning the heads to the proper track for adjustment should be performed at the Sorbus Repair Center/Sorbus Station only. To position the heads use BB/M and the GET directive. Use the following commands:

```
DIM A$ (256)
GET D, T*32+H,A$
```

D=Disk, T=Track, H=0 (upper head), H=16 (lower head)

Examples:

To position the heads to track 32, Head 0: GET D, 32*32,A$
To position the heads to track 32, Head 1: GET D, 32*32+16,A$

4.5.1.8 Disk Drive Compliance Measurement

To measure compliance perform the following steps in the order listed:

1. Apply power to the disk drive and select drive.
2. Step head(s) to track 79.
3. Write a 1F pattern (62.5 KHz) on the entire track.
4. Connect oscilloscope probes to TP1 and TP2 as in radial track alignment procedure (refer to paragraph 4.5.1.1).
5. Apply a 15 gram load to the upper arm directly above the load pad. If the amplitude observed on the oscilloscope increases by more than 10% the drive has poor compliance; refer to troubleshooting information in paragraph 4.6.8.

4.5.1.9 Disk Drive Erase Measurement

To measure the effectiveness of the erase, perform the following steps in the order listed.

1. Apply power to the disk drive and select drive.
2. Step the head(s) to track 64.
3. Write a 1F pattern (62.5 Kilohertz) on the entire track.
4. Connect oscilloscope to TP1 and TP2 as described in radial-track alignment procedure (refer to paragraph 4.5.1.1).
5. Connect a jumper from ground to gate 6A pin 7 (Model 91/92 bottom head) or 6A pin 1 (Model 92 top head).
6. Step back and forth across track 64 for about 15 seconds.
7. At the end of the 15-second period, remove jumper installed in step 5 above, return head(s) to track 64. The amplitude displayed on the oscilloscope should be reduced by at least 85% in some parts of the trace.
8. If the amplitude decrease is less than 85%, refer to the trouble-shooting information, (refer to paragraph 4.6.8).

4.5.1.10 Disk Drive High Frequency Playback Measurement

To measure the amount of high frequency playback, perform the following steps in the order listed.

1. Apply power to the disk drive and select drive.
2. Step the head to track 79.

3. Write a 2F (250 Kilohertz) pattern on the entire track.

4. Connect oscilloscope to TP1 and TP2 as described in radial-track alignment procedure (refer to paragraph 4.5.1.1).

5. The peak-to-peak amplitude displayed on oscilloscope should be a minimum of 65mv p-p. If the amplitude is less than 65mv p-p, refer to the troubleshooting information (refer to paragraph 4.6.8).

4.5.2 Video Display Adjustment

Periodically the video display requires adjustment and alignment because of component aging on the Video assembly, minor knocks to the unit, or CRT replacement. To align and adjust the display, proceed as follows:

WARNING

Improper adjustment of the video circuits may result in an X-ray radiation hazard. Refer to the video monitor instruction manual.

1. Turn on the S/10 and set it to Local mode.

2. Set the screen for normal video and clear it of any data (Function/Home and Function/EP).

3. Press and hold CONTROL and press Up Arrow repeatedly to set the screen to maximum intensity.

4. Reduce the ambient lighting to a level that would make reading uncomfortable, or shield the screen as much as possible from the ambient lighting if reducing it is impractical.

5. Adjust BRITE R207 on the Video assembly until the raster and retrace lines appear on the display, then back off to the point where they disappear.

6. Return the ambient lighting to normal.

7. Set the display to 132-column (FUNCTION/80/132) mode and press ESCAPE#8 for the E test pattern.

8. Adjust VERT SIZE R307 on the Video assembly for the maximum display pattern height.

NOTE

When adjusting the display vertical size, allow for parallax at the top of the screen when viewing the screen from a normal typing position.

9. Adjust R204 FOCUS on the Video assembly for maximum edge sharpness on the screen.

NOTE

Focusing hint: type a few lines of lower case m's at the display top, center, and bottom, then adjust the display for the maximum definition of these characters.

10. Adjust T101-HORIZONTAL OSCILLATOR COIL on the Video assembly to center the test pattern on the screen. Ensure that no foldback occurs at the left or right display edges (see figure 4-6).

11. Return the S/10 to normal operation.

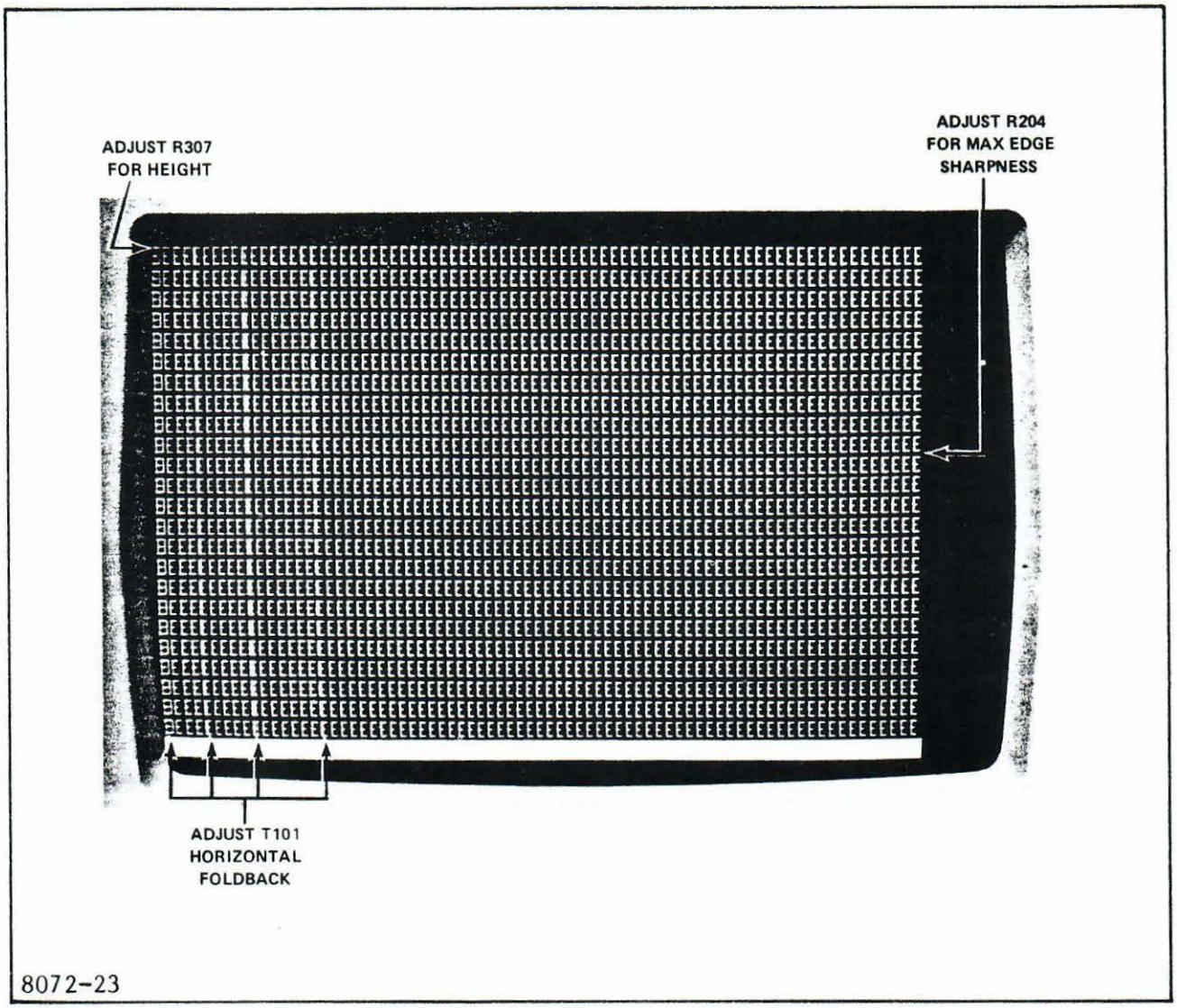


Figure 4-6. E Test Pattern

4.6 SYMPTOM AND FAULT ANALYSIS

Before isolating faults in the S/10 review the system block diagram and its description in Section III of this manual.

4.6.1 S/10 and Office Display Trouble Analysis

Before swapping assemblies when a problem is suspected, take some basic troubleshooting steps first. These steps should include carefully analyzing the fault symptoms and comparing them against normal operating indications.

Basic, logical troubleshooting steps apply as much to the S/10 as to any other electronic equipment. To analyze a suspected fault, proceed as follows:

1. Recognize the symptoms. Review the symptoms of the problem complaint. Try to duplicate the symptoms by operating the S/10 in the same manner as when the symptoms first occurred; that is, verify the symptoms.

2. Look for other symptoms. Check the S/10 for other symptoms that may be caused by the same fault (for example, by testing other operational modes).

3. Select likely faulty areas. Consider which functions or assemblies, including operator actions, may be causing the symptoms. The fault may be as simple as the incorrect use of an Escape or Control Sequence (refer to the User's Guide).

4. Isolate the faulty function or area.

5. Go to the troubleshooting table (refer to table 4-1) and find the symptoms to further isolate the fault to an assembly.

Due to the integral nature of the hardware and software of the unit, it is sometimes difficult to determine whether a problem is hardware or software related. The easiest method to determine this is to place the module that contains the memory section into another unit and perform the same test that made it fail in another unit. If the memory section is at fault, the problem will exhibit itself in the new unit.

The personality of the unit contains a self-test that checks the EPROMs by performing a checksum. If an error occurs in this test, the unit will display a quote (") error in the first field of status line one (1) or will display ROM ERROR in the status line, depending on the product model. The self-test also does a check of the NVR and will indicate an error with an exclamation point (!) in this same position (or will display NVR error in the status line). If both of these errors have an error, a pound sign (#) will be displayed.

An NVR error will cause the unit to power up with default NVR settings. The obvious symptoms are a power up in LOCAL with baud rates set at 9600. Occasionally the NVR will lose its settings and will appear as an error, when in fact a Function/(Control) Save will clear the problem.

4.6.2 Advanced Video Processor (AVP) Troubleshooting Aid

There are eight major circuits that comprise the terminal portion of the AVP units. The total circuit should be repaired in steps. The steps are outlined below. The reason for troubleshooting in steps is the sequence in the way data passes through the terminal circuitry. An apparently simple problem may be nearly insolvable if the previous sequence is not functioning properly. The screen is not a useful indicator of a problem until the clocks and the DMA are working.

The eight sequences are:

a. System clocks (Schematic page 2) - System clocks are initiated by a 18.432 MHz crystal. There are many clocks that are generated by dividing the 18.432 MHz frequency with flip-flops and interruptable counters. The slowest of the clocks is the vertical clock pulse. Vertical blank is 60 Hz and must be working for the other major circuits to function. Use vertical blank to determine if the clocks are functioning properly. Generally, if vertical is correct the rest of the clock circuits are working. If there is any doubt scope the clock that is in question.

b. DMA and memory circuits (Schematic page 5) - The DMA is the most difficult circuit to diagnose. This in part because the memory has to be working and in part because certain portions of the Z80 circuits have to be working. The hub of the DMA is a 74S151. It is strongly recommended that this device be reviewed in a TTL Data manual. The DMA has a set of PROMS that are addressed by a 2911 sequencer. The PROMS provide control data to the memory, the Z80 circuits, and the line buffer. The 74S151 is used to interrupt the 2911 sequencer. This makes knowledge of the 74S151's operation very important.

   Lost or extra interrupts are the primary causes of DMA failures. If you suspect a memory failure, the fastest way to find it is to scope the RAS and CAS circuits. If they are okay try the WE circuit; if it is okay verify that all of the address lines are switching. The next step is to verify the data in and out of each memory device. Generally, if all of the inputs to the 74S151 are switching properly (a working spare for comparison is a necessity) the problem is Z80 related. The Z80 device itself is very reliable. Most Z80 related failures come from external sources such as Bus Request, Reset, Interrupt, I/O Reg and erroneous data and address bits.

c. Z80 (Schematic page 1) - The Z80 is a straightforward processor with eight data bits and sixteen address bits. As was previously indicated the Z80 is a very reliable device. The majority of Z80 problems are externally generated. It is highly recommended that the Z80 data book be reviewed. Many problems can be solved by observing the incorrect Z80 outputs and checking the data sheet to determine the cause. Proper Z80 operation is dependent on proper DMA and memory operation. Beware that the Z80 (and many other devices in this circuit) are Tristate devices: an output that is neither high nor low is not necessarily defective.

NOTE

The schematic page also shows the CPU and Printer Port circuits. Unless you determine that they are effecting the Z80 operation do not attempt to operate them until the screen is working. The same applies to the keyboard.

d. Line Buffer (Schematic page 3) - The purpose of the line buffer is to select the proper information from the data bus and to decode it and prepare it for presentation on the screen. The decoded information determines where it will appear on the screen, what video attributes will be used, cursor location, as well as what data appears on the screen. The line buffer maintains line count and video dot count in its own memory. The line buffer memory retains all of the screen information during each sweep of the screen. The Line Buffer is reloaded by the Z80 each time the screen is swept.

Memory addressing is provided by interruptable counters (74163s). If the line buffer memory is working properly the address counters will select the proper data to maintain the characters that are displayed on the screen. The memory also contains the video attribute and feature information that is contained in the display. The other major information that is stored in line buffer memory is the XY location of the data that is to be presented.

NOTE

The data or the pattern on the screen may or may not have any validity when the problem is in the line buffer. If there is a problem in the Clock, DMA, or Z80 circuits, the screen has no validity.

e. Video Output (Schematic page 4) - The video display consists of circuits that store the character fonts, convert the parallel data to serial data, merge the video attributes, and an analog circuit to present the information to the video sweep circuitry.

NOTE

The video electronics portion of the terminal requires three signals from the AVP. They are horizontal retrace, vertical retrace, and video. Only video comes from page 4.

An important part of the video output circuitry is circuits that address the font memory. The font memory does not store entire characters. The display is dot matrix oriented and the font memory stores individual dots. The memory address timing is the dot rate timing. This means that during each horizontal sweep every dot across the screen has a font memory address. It should be noted that the video display assembly is interrupted by the horizontal and vertical retrace signals.

f. Font Load (Schematic pages 3 and 4) - It is possible to have a properly managed screen with an operational keyboard and no video characters. In most units the font is downline loadable. The fonts are stored in a pair of 24 pin memory IC's. These memories are pin compatable with 2716 EPROMS and if the downline loadable feature is not included EPROMs will be used. The font load feature occurs following a reset or an escape sequence from a host computer. There are test PROMs that continually repeat the font load sequence and they should be used if the font load is failing. Font loading is accomplished by decoding Z80 instructions in the line buffer. When the line buffer has decoded the font load instructions, it loads the data which follows into the font memory. There are no write enable pulses after the font load is complete and the terminal returns to normal operation.

g. Keyboard (Schematic page 1) - The keyboard communicates with the terminal in serial mode. The AVP has a resistor diode network that pulls up the keyboard input to the proper levels to input to an 8251A USART. The USART converts the serial input data to parallel data and presents it to the CPU via interrupt mode. Keyboard information is primarily one direction, the only exception is keyboard reset which is accomplished by turning off keyboard power. There are no data output signals to the keyboard.

Troubleshooting the keyboard is straightforward, the first thing to check is the hookup: the keyboard must be properly connected. The second check is the clock to the USART. The next step is to check the interrupt line at pin 14 of the USART. The USART is socketed and is easy to replace. This is a quick way to check its condition. The only other possible causes of keyboard input failure are external from the keyboard circuit and the rest of the board circuits should be rechecked. If pin 14 of the USART pulses when a keystroke occurs, but the keyboard input does not work, check pin 16 of the Z80. There should be a screen interrupt that occurs at vertical frequency and a keystroke interrupt.

NOTE

Different units may use different keyboards but when test 24 is used the operation will be the same.

h. I/O Ports (Schematic page 1) - The I/O Ports are microprocessor controlled. The circuitry is complex in the way it operates but it is not complex to trouble shoot. The majority of field problems are due to improper voltages being supplied up to the I/O ports. This will damage either or both of the 1488, 1489 line drivers. The rest of the circuit is plugged into sockets and the easiest fix is to try a replacement part.

NOTE

Many I/O port problems are reported that are cable or improper hookup problems, i.e., a shorted cable or not all of the wires are in the cable. Verify that you really have a problem with a known good I/O device and a known good cable, a second terminal is ideal.

The steps outlined above deal with screen management and terminal operation. There is also an NVR circuit which has the capability of retaining unique information when the terminal has been turned off. The problem may be the NVR device itslef or the input/output circuits that feed it. These appear on page 5 of the schematics.

The NVR uses a unique -28 volt input. Before any other troubleshooting is done check pin 14 of the NVR IC for -28V. The -28V is generated on the AVP by a small switching power supply that consists of a transistor, a cap, a choke, two zener diodes, and bias resistors. The switcher operates on -12 volts.

The steps outlined are intended to assist in troubleshooting the AVP. It should be remembered that the AVP is a complete terminal logic board. Problems with floppy type units are AVP problems only when the terminal portion of the unit is failing. The problems are not readily discernable if the board is plugged into a unit. A test fixture and an oscilloscope are necessary.

The AVP board is laid out on a grid using numeric characters to designate the columns and alpha characters to designate the rows. The assembly has most of the IC locations silkscreened on the board. The discrete components are numbered, i.e., C1, R3, Q2, CR5. There are approximately 70 filter capacitors that are not numbered. They should be all .1 microfarad. To locate a numbered discrete component look for the ICs it is attached to and it will be in the immediate area.

Learning to effectively test and repair AVPs requires several oscilloscope techniques. Wave form analysis is important as well as timing relationships. One of the major uses of an oscilloscope is pattern analysis. There are several long trains of pulses that can tell the user a considerable amount about the condition of the circuit. The only way to fully understand the patterns is to observe them one or two at a time.

The test procedure with this aid has a list of test points that should be observed using a good AVP. This is an invaluable aid to determine how much of the board is working and how much is not. Several of the test points have to be observed at a very slow sync rate, i.e., 2 milliseconds. The test operator should be familiar with delayed sync oscilloscope techniques.

4.6.3 Advanced Video Processor Test Procedure

Determine the configuration of the AVP to be tested, i.e., 16K, 64K, downline loadable font, etc. Insert a TEST 24 EPROM in the first EPROM location.

Use TEST 24 (refer to paragraph 4.6.4) to determine if the board is operating properly. All of the features and the data pattern used in TEST 24 should be observed on a working board before you start. If the data pattern is correct, test the keyboard input and verify that the correct data appears on the bottom line of the screen. The right arrow on the keyboard will set 132 column mode. The test pattern should be the same with the exception of smaller characters. If the 80 and 132 characters are ok press PF7. A different pattern will appear and this is an NVR test. PF1, PF2, PF3, and PF4 will each write and verify a different data pattern in the NVR. A failure is designated by an underline and the two different data patterns will appear in HEX. If the test was successful, all of the data patterns will match and the checksum will match.

When all of the TEST 24 operations are correct and complete power down and remove the TEST 24 EPROM and insert the correct firmware for the final configuration of the PCBA. If the board is to be used in a terminal type unit, apply power and the screen should show a cursor and a status line. The status line will say ! Local. There are 4 displaying status lines and a blank status line. These may be observed by entering a FUNCTION 4 on the keyboard. Set all of the status lines the way the operator will be expected to use them. After the status lines are entered press FUNCTION, CONTROL and S. The status line will say Wait. After the wait message goes away, reset the unit by pressing FUNCTION BACKSPACE.

If the unit is working properly the information you entered in the status lines will be saved. If not return to TEST 24 and retest the NVR circuit. If the board is to be used in a floppy unit plug an AFC in the other test connector and attach a floppy disk drive to the unit. Load a diskette with a loader program and the screen should come up with the same information as a terminal screen. The rest of the testing will be the same.

The next step after the screen is correct is to test the two I/O ports. The port nearest the corner of the board is the main port; the other is the auxiliary port. The best way to test the ports is to attach a cable to another working terminal. Attach an RS-232C cable to the auxiliary port of one terminal and to the main port of a second terminal. Put the sending unit (the unit with the cable in the auxiliary port) in LOCAL and the receiving unit in LINE mode. Fill the screen with data and press the FUNCTION PRT keys. The data should appear on the other screen.

NOTE

The top line will scroll off of the screen;
the last operation of the print operation
is a line feed.

If this test is successful, press the FUNCTION CPY keys and enter data from the keyboard. The data will appear on both screens. Switch the cable and repeat the test.

4.6.4 TEST 24 Diagnostic

The TEST 24 EPROM is used to perform basic diagnostic functions using the CRT screen and the standard keyboard. Besides stabilizing the circuit for more indepth repair using an oscilloscope, this diagnostic can pinpoint circuit sections to begin tracing a malfunction. The following outline describes the setup procedure and the functions that specific keyboard keys perform. The second section gives a description of the EPROM output and which high suspect circuits to investigate.

4.6.4.1 Setup

The EPROM is a stand alone test that does not require any other firmware or software.

The configuration is a standard terminal with the memory module being configured as appropriate.

4.6.4.2 Key Functions (Standard Keyboard Only)

The DIAGR performs several functions using keyboard keys. Most of the specific key functions are toggles. Those keys and their functions are:

PF1 - Reverse video screen, same as FUNCTION/SCREEN

PF2 - Block or underscore cursor, same as FUNCTION/CURSOR

PF3 - Turns Bell on or off

PF4 - Complement display all function (FUNCTION/M). (HARDWARE DEPENDENT)

PF5 - NVR Write

PF7 - Performs a reset

SCROL UP- Raise screen intensity

SCROL DOWN - Lower screen intensity

PAGE LEFT - 80 character font

PAGE RIGHT - 132 character font

PF8 - Sets up the NVR test after PF7 is set. PF1, PF2, PF3 and PF4 will write and verify four different data patterns in the NVR circuit.

Besides the specific key functions, keyboard input is also allowed. When the keyboard is used, the FUNCTION, HOLD and KEYPAD keys are disabled. The keyboard output can be seen on the bottom line of the screen.

4.6.4.3 TEST 24 Output

The output of TEST 24 exercises 85% of the terminal's capabilities. Lines of data are displayed on the screen in any of the various configurations that can be displayed by the terminal. The display will contain all the features and video attributes that the terminal is capable of performing.

4.6.4.4 Keyboard Test

When connecting and disconnecting the keyboard, a click should be heard. If this click is not present, the keyboard is most likely not outputting to the terminal or the terminal is not recognizing keyboard input. This may also indicate that no power is being suppled to the keyboard.

TEST 24 has the capability of testing 85% of the terminal circuitry. The oscilloscope patterns that were referred to in the previous test and trouble-shooting sections are best observed using TEST 24.

4.6.4.5 TEST 24 Detail

TEST 24 is designed to aid the technician in diagnosing the Advanced Video Processor (AVP) employing either the FONT ROM or FONT RAMS (if the AVP is properly set-up). TEST 24 operates with all interrupts enabled and serviced in a manner which is similar to how a terminal personality handles them.

4.6.4.6 Initialization

Before the interrupts are enabled, the following will occur.

a. RAM is allowed to come-up and start operating properly.

b. CTC1 and the DART are set-up.

c. CTC2, which is on the floppy controller board, is disabled.

d. Data for the primary diagnostic and its associated tables is moved from ROM to high RAM, where the DMA may access it.

e. The FONT data and tables are moved from the ROM to RAM.

f. A simple compare is made between some of the data in RAM and its source in ROM to check for bad RAM. If a bad compare is made, a message will be placed on the top line of the screen and the bell will be garbled. The bell may be disabled by pressing PF3.

g. A memory sizing test is made to determine whether 16 or 64K of RAM is present.

    1. If the bytes at 08000H and 0C000H are not equal then 64K of memory is assumed.

    2. If the bytes at 08000H and 0C000H are the same, the byte at 8000H is complimented and written back to that location. 0C000H is then read and compared to the byte at 08000H and if they are the same, 16K of memory will be assumed.

h. The keyboard is enabled and the keyboard entry line is set-up.

i. A check is made to determine whether the diagnostic is operating out of RAM, and if it is a bit will be set in the cursor control port.

j. The interrupts are then enabled allowing the fonts to be loaded after 255 normal screen interrupts, which allows the character generator and associated circuitry to become stable. The long time period, also, allows the technician to check the screen pattern before load font in case there is a load font problem.

4.6.4.7 Normal Execution

After the interrupts are enabled, keyboard commands or data may be entered.

a. Pressing any alpha-numberic key will result in that character being displayed on the keyboard data line, approximately one-third of the way down the screen. Each character forces a video attribute and the character depressed to be entered in the data line.

b. Screen brightness may be controlled by depressing the scroll up and down keys. This forces a new value to be output to the video intensity control port.

c. 80 and 132 column mode may be switched by depressing the page back (for 80) and the page forward (for 132) keys. This forces the appropriate character attributes to be written to the video display table stored in RAM.

d. PF1 will reverse the screen from white on black to black on white by toggling the screen background bit in the video control port.

e. PF2 compliments the cursor style from a block style to the underline cursor by toggling the cursor style bit in the video control port.

f. PF3 controls the bell by toggling a bit in the video control port. PF3 will also terminate the warning warble which is activated by bad RAM or a bad SIO test.

g. PF4 toggles a bit in the video control port which tells the video controller to display or hide attributes on the screen.

h. PF5 causes the hardware to perform a cold boot if it was downloaded into the terminal memory from the floppy system, otherwise, it will act as a reset identical to PF8.

i. PF6 does a simple test on both the primary and secondard ports. A R232 cable (with pins 5 and 20 swapped) is connected to the primary and secondary RS232 connectors on the AVP and the PF6 key depressed. Data will be transmitted from the primary port, while the secondary port listens and compares the received data to the data that was sent. If bad data is found, a message will be placed in the top line on the screen and the bell will be warbled, terminating the test. The bell may be silenced by depressing PF3 once. If all comparisons are correct in one direction the data flow is reversed and the test is performed again. Any interrupts caused by CTS or DTR or by any receive errors will cause the error condition to be enabled. If the complete cycle is not completed within three seconds the error condition will again be raised.

j. PF7 will cause TEST 24 to start executing a secondary diagnostic which will allow the technician to select a test pattern to be written to the NVR and then read back. A compare will be made between the data read and the data written with any errors flagged on the screen. PF8 will do a total reset within the diagnostic and bring command back to the main screen.

k. PF8 does a hard reset which will perform the same initialization as a power-on reset.

1. After the execution of any of the above keys, TEST 24 will go back into a loop which checks the keyboard buffer full flag, waiting for the next key to be pressed.

4.6.4.8 Line 25 Interrupt Servicing

The DMA causes an interrupt 60 times every second, requesting a new video display table (VDT) RAM address from the Z80. The Z80 honors this interrupt request by passing back to the DMA the VDT address through two ports (low order address passed first). Additional functions performed during LINE 25 are:

a. The keyboard USART will be checked to see if any data had been entered since the last LINE 25 interrupt. Any valid data will be placed into the keyboard buffer and the associated flag set to tell the execution loop that a character is ready. If a character is found to be in error, the USART error will be cleared and the data thrown away.

b. A new cursor position is written to the flying cursor.

c. Cursor and screen blinking must be handled by checking the current value, updating it, and outputting a new value to the cursor control port, if needed. The cursor toggles either on or off every sixteen LINE 25 interrupts, with the screen rate at every thirty-two interrupts.

d. A byte in memory is checked to determine whether the load font table address should be passed instead of the normal VDT address. When the font load table is passed, the DMA will attempt to load into the FONT RAM the font data needed to display the characters on the screen. If the FONT RAM is present, the DMA will unsuccessfully attempt to write over the data.

e. A check will be made to determine whether a RAM or SIO error has occurred. If it has a bell, counter will be incremented and the bell may be turned on or off depending on the count.

4.6.5 Advanced Floppy Controller (AFC) Troubleshooting Aid

The AFC consists of two circuits on one PCBA. One circuit is the floppy controller and the other is a CPU with a dedicated 64K memory.

A working AFC will cause the two floppy drives to alternately search for a diskette. When the floppy controller finds the diskette it will read the operating system into the processor memory and interrupt the terminal. The terminal interrupt will cause a terminal personality to be loaded into the terminal memory. After the terminal personality is loaded a standard screen will appear. It is recommended that the technician trouble-shooting an AFC PCBA remember the separate functions of the two 64K RAM circuits.

a. CPU and Memory (Schematic page 1) - A failing unit will not complete some portion of the load sequence. The memory is key to the AFC operation; a failing memory will cause both the CPU and floppy controller portions of the AFC to not work. The first step is to check the RAS and CAS lines. These have to be working for the memory to operate. The memory is addressed in part by a PROM set. Verify that the PROM set is working. The Z80 clock is developed by a PAL (programmable array logic unit). The PAL also develops RAS, CAS and WE. If all of the control and address lines are functioning, check the data input and output lines. If these are incorrect, the problem may by a RAM IC. The RAM is initialized by a 16K EPROM. This is accomplished by disabling the RAM output and enabling the EPROM output. During the time the EPROM is enabled the start sequence is transferred to RAM and the firmware disables the EPROM and enables the RAM output.

b. Floppy Controller (Schematic page 3) - If the memory and CPU are working properly, go to page 3 of the schematic and check the operation of the floppy controller IC (a data sheet for the floppy controller is included in the Reference Data). The floppy controller should be receiving data from the Z80. This data is the commands that cause the floppy controller to read or write to the disk. There is an analog circuit that is used to synchronize the disk drive with the controller. The VCO (voltage controlled oscillator) is programmatically started at a very slow rate that gradually increases to 250K Hz and syncs with the disk. The clock for the floppy controller is generated by a 8 MHz crystal and divided by a 74LS163 counter. The data path for data and index are important places to look for proper operation. Commands to the floppy are driven by a 74S240, and they are easy to verify.

c. 32 Bit Port (Schematic page 2) - If the CPU, memory, and floppy controller appear to work but the data does not transfer to the terminal properly, go to the schematic page 2. There are two Z80 CTC ICs on this page. The one located at 13D is used by the terminal Z80 and the one at location 13B is used by the AFC Z80. The Z80 CTCs are used for interrupt management., All interface between the Z80s is done in interrupt mode. The transfer of data is accomplished by 4 74LS670 ICs, these devices are 4 x 4 bit buffers and the circuit is referred to as a 32 bit port. Up to 4 bytes of data can be stored in the buffer on a first in first out basis. It is recommended that you refer to the Z80 data book and a TTL manual if you suspect a problem with this circuit.

4.6.6 Advanced Floppy Controller Test Procedure

This procedure is intended to verify the operation of an Advanced Floppy Controller PCBA.

1. Plug the board to be tested into a standard S/10 with an AVP in the processor slot. Apply power, and with an oscilloscope verify that SEL0 and SEL1 are switching approximately once per second.

2. Power down the test fixture and connect the two floppy drive connectors. Power up the unit and the floppy drive should be starting and stopping approximately once per second. Insert a diskette with a CP/M system installed and close the floppy door. The system should start to read the diskette. When the load is complete a standard screen will appear.

3. Enter DIR and press RETURN. The directory for the diskette should appear. Load the FORMT program and verify the format on the diagnostic diskette.

NOTE

All diagnostic diskettes should be write protectd. After the format verifies successfully, attempt to format the diskette. A write protect message should appear on the screen. Restart the format program and attempt to read the format with the disk drive door open, the error message should tell you the door is open.

4. Restart the FORMAT program and put a blank diskette in the drive and format it.

NOTE

This is the first time the system has tried to write; most write problems are with the 8 MHz oscillator.

4.6.7 Troubleshooting Chart

Table 4-1 is a Troubleshooting Chart that list symptom, probable cause, and corrective action. The Troubleshooting Chart should be used as a quick aid in locating probable cause of normal failures.

Table 4-1. System S/10 Troubleshooting Chart

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Unit does not power up	No power applied	Check outlet/power cord; replace cord if necessary
	Blown fuse	Replace the fuse; find out why it blew
	Line filter	Check input/output; replace filter if required
Unit hums, emits constant chirping	Power Supply	Check input/output; replace if necessary (refer to paragraph 5.2)
	Power Start	Check cables to floppy drive assembly.
	Disk Drives	Replace the disk drive (refer to paragraph 5.10)
Unit beeps at power on, but no display	Flyback transformer	Replace transformer (refer to paragraph 5.4)
	Video board	Replace video board (refer to paragraph 5.3)
	CRT	Replace CRT (refer to paragraph 5.6)
Keyclick/bell tone missing	Not selected	Turn on at keyboard
	Bad speaker	Replace speaker (refer to paragraph 5.9)
	Broken wire	Check continuity; repair or replace wire
	*Advanced Video Processor	Check speaker output and replace as necessary

*The Advanced Video Processor (AVP) Board is different configuration for ODT and system S/10. Refer to Section VI, Parts List

Table 4-1. System S/10 Troubleshooting Chart (continued)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Flashing or intermittent characters on display	*Advanced Video Processor	Reseat circuit assemblies
		Reset the unit
		Power off; power on
	Bad disk	Try another disk
	Bad drive	Check the disk drive
No communication with host computer	Interconnect cable	Check all cables
	Hold in effect	Release HOLD key
	Unit in Local Mode	Put unit in Line Mode
	*Advanced Video Processor	Check output; replace as necessary
	Port assignment not set or wrong baud rate	Display status line or set up menu. Set correct settings
Fails to perform a SAVE operation	Non-Volatile RAM (NVR)	Replace NVR or board #2 (refer to paragraph 5.1)
Distorted display	Video board	Check input/output; adjust/ replace as necessary (refer to paragraph 5.3)
	Power supply	Check input/output; adjust/ replace as necessary (refer to paragraph 5.2)
Characters folder over at edge of display	Video board	Adjust horizontal/phase pot
Display too high or low	Video board	Adjust vertical size pot

*The Advanced Video Processor (AVP) Board is different configuration for ODT and system S/10. Refer to Section VI, Parts List

Table 4-1. System S/10 Troubleshooting Chart (continued)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Display too dim or bright	Video board	Adjust intensity pot
	Wrong setting	Set from keyboard and SAVE in NVR as required
Display out of focus	Video board	Adjust focus pot
Solid horizontal or vertical line on display	Video board	Replace video board (refer to paragraph 5.3)
Missing characters	Wrong baud rate set	Set to correct baud rate
	Wrong parity set	Set correct parity
Rubout/DEL characters displayed	No handshake protocol set	Check system manual; set host for XON/XOFF or set lower baud rate
	Parity error	Set correct parity
	In Monitor Mode	Select correct operating mode
No keyboard interaction	Keyboard cable	Check keyboard cable
	Keyboard	Replace keyboard
	Keyboard USART	Replace AVP/Replace keyboard PCBA
Fan doesn't turn	No power	Power not connected
		Power supply not fully inserted
		Disk drive not properly connected
	Broken wire to fan	Repair or replace wire
	Board #2 Controller Board	Check output, replace if necessary
	Defective fan	Replace fan

*The Advanced Video Processor (AVP) Board is different configuration for ODT and system S/10. Refer to Section VI, Parts List

Table 4-1. System S/10 Troubleshooting Chart (continued)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Fan turns, drives do not	Drive connectors not properly inserted	Check all connections
	Controller	Replace board #2 (refer to paragraph 5.1)
	Defective drive	Replace disk drive (refer to paragraph 5.10)
Both drives turn continuously	Ribbon connector reversed	Check all connections
Drives turn alternately, but system will not bootstrap	No diskette	Load a system diskette
	Bad diskette	Try another diskette
	Drive not aligned	Try the other disk drive (refer to paragraph 4.6.8)
	Defective disk interface	Replace board #2 (refer to paragraph 5.1)
	Defective processor board	Replace board #1 (refer to paragraph 5.1)
Some programs will not run	Damaged diskette	Try another disk drive (refer to paragraph 4.7.6.3)
		Try another diskette
	Drive misaligned	Refer to paragraph 4.5.1 for alignment
	Defective drive	Refer to paragraph 4.6.8
	Defective drive interface	Replace board #2 (refer to paragraph 5.1)
Video not framed	Video board not adjusted	Make adjustments (refer to paragraph 4.5.2)

*The Advanced Video Processor (AVP) Board is different configuration for ODT and system S/10. Refer to Section VI, Parts List

Table 4-1. System S/10 Troubleshooting Chart (continued)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Display has jitter, rolling, etc.	Defective video board	Replace video board (refer to paragraph 5.3)
	Defective *Advanced Video Processor	Replace board #1 (refer to paragraph 5.1)
	Defective power supply	Replace power supply (refer to paragraph 5.2)
Screen unmanaged, keyboard locked out	Defective *Advanced Video Processor	Replace board #1 (refer to paragraph 5.1)
	Defective drive interface	Replace board #2 (refer to paragraph 5.1)
The following symptoms pertain to the CRT Video Amplifier circuit board and power supply.		
No Video at all	Video Generator Module or Video Board or Power Supply or any combination of the above	Check voltage from Power Supply at pin 7 of the plug connecting at the top of the Video Board. Pin 1 is to the back of the system. Voltages should be approximately 12 VDC. No voltage indicates a bad Power Supply Check pin 6 of the same plug for a 2 volt peak-to-peak signal of approximately 15.750 Hz. If no signal is there, replace the Video Generator Module Check pin 8 of the same plug for approximately 1.5 volts peak-to-peak signal. If no signal is present, replace the Video Generator Module.
Thin horizontal or vertical line on video screen; no video elsewhere on screen	Deflection coil	Replace Deflection Yoke

*The Advanced Video Processor (AVP) Board is different configuration for ODT and system S/10. Refer to Section VI, Parts List

Table 4-1. System S/10 Troubleshooting Chart (continued)

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Thin vertical line	Q306/Q307 on Video Board	Replace Q306 or Q307 and with power off and blue and white wires disconnected, check continuity across deflection coil where blue and white wires are hooked up. An open, or high resistance, indicates a defective deflector coil
Thin horizontal line	Q104 on Video Board	Replace Q104 and with power off and yellow and red wires disconnected, check continuity between the points that the yellow and red wires are connected to. An open or high resistance, indicates a defective deflector coil
Video is off center on screen	Video Centering Magnets on deflection coil need to be adjusted	Adjust Video Centering Magnets for best centering of video on screen (remove all jewelry and use caution, remember, the system is on
Bad focus	R204 of the Video Board needs to be adjusted	Adjust 204 as necessary for sharpest focus. Be careful not to short the adjustment tool to other components
Insufficient brightness	R207 of the Video Board needs adjusting	Adjust brightness on front bezel of the computer to mid-travel then adjust R205 of Video Board to desired screen brightness
No Sync on screen no horizontal or vertical hold	Video Generator Module (VGM)	Replace U11 (Video Controller). If the problem is not corrected, replace VGM
Jittering of video and intermittent dropping out and reappearing of video dots on the screen	High voltage leak or leaks	With power off and capacitors discharged, check high-voltage leads for breaks, kinks or placed too close to motherboard brackets. Position wires toward the Video Board and away from the motherboard area. Also, bad CRT's have been known to cause this symptom.
Video Board has been replaced and still have no video	Video Generator Module (VGM)	Replace U4 (74LS86) and U15 (74LS11)

4.6.8 Disk Drive Trouble Analysis (S/10 Only)

This subsection contains general troubleshooting information for the Disk Drive. The first step in troubleshooting the drive should be to verify that the controlling device and interface to the disk drive are functioning properly. Next, isolate the trouble to the electronic, the electromechanical, or the mechanical components of the drive. Table 4-2 is a list of some trouble symptoms referenced to paragraph steps which include possible causes and suggested fixes.

Table 4-2. Disk Drive Trouble Symptoms

TOPIC	PARAGRAPH
Preliminary Troubleshooting Steps	4.6.8.1
Drive Won't Step or Steps Erratically	4.6.8.2
Head/Carriage Oscillates at Track 00 (Restore Error)	4.6.8.3
Drive Motor Won't Rotate	4.6.8.4
Head Will Not Load	4.6.8.5
Bad Index Output	4.6.8.6
Bad Write Protect Output	4.6.8.7
Activity Indicator Does Not Light	4.6.8.8
Read Errors - All Tracks	4.6.8.9
Read Errors - Random Tracks	4.6.8.10
Read Errors - Inside Tracks	4.6.8.11
Cannot Read Prewritten Data: Can Read Self-Written Data	4.6.8.12
Cannot Write Data	4.6.8.13
Erase Bad	4.6.8.14
Drive Speed Unstable	4.6.8.15

4.6.8.1 Preliminary Troubleshooting Steps

The following preliminary steps should be performed first when a suspected malfunction occurs:

1. Check for proper operation of controlling device and interface to disk drive.

2. Check for proper supply voltages to the printed circuit board assembly (PCBA); refer to Section III.

3. Check for proper insertion of programmable shunt and terminator.

4.6.8.2 Drive Won't Step or Steps Erratically

Verify that head cable(s) do not interfere with carriage movement.

1. With DIRECTION input low, apply stepping pulses and monitor stepper motor control logic for proper signals as shown by timing diagram, figure 4-7.

2. In order to step, the following circuit points must be at the levels indicated:

   a. Counter 3C pins 7 and 10 must be low.

   b. Counter 3C pin 9 must be high.

3. If signals measured are as shown by figure 4-7, replace the stepper motor.

4.6.8.3 Head/Carriage Oscillates at Track 00 (Restore Error)

1. Position the head/carriage to extreme rear of drive.

2. Check J4-12 for a low level. If it is not low, replace the track 00 sensor.

3. Check track 00 logic for correct signals.

4.6.8.4 Drive Motor Won't Rotate

1. Signal MOTOR ON must be a low level for drive motor to rotate.

2. Short together the collector and the emitter of output driver Q3. This should cause the drive motor to rotate at full speed, generating a TACH signal. If drive motor does not rotate, replace it. Check the drive motor logic and compare with timing diagram, figure 4-8.

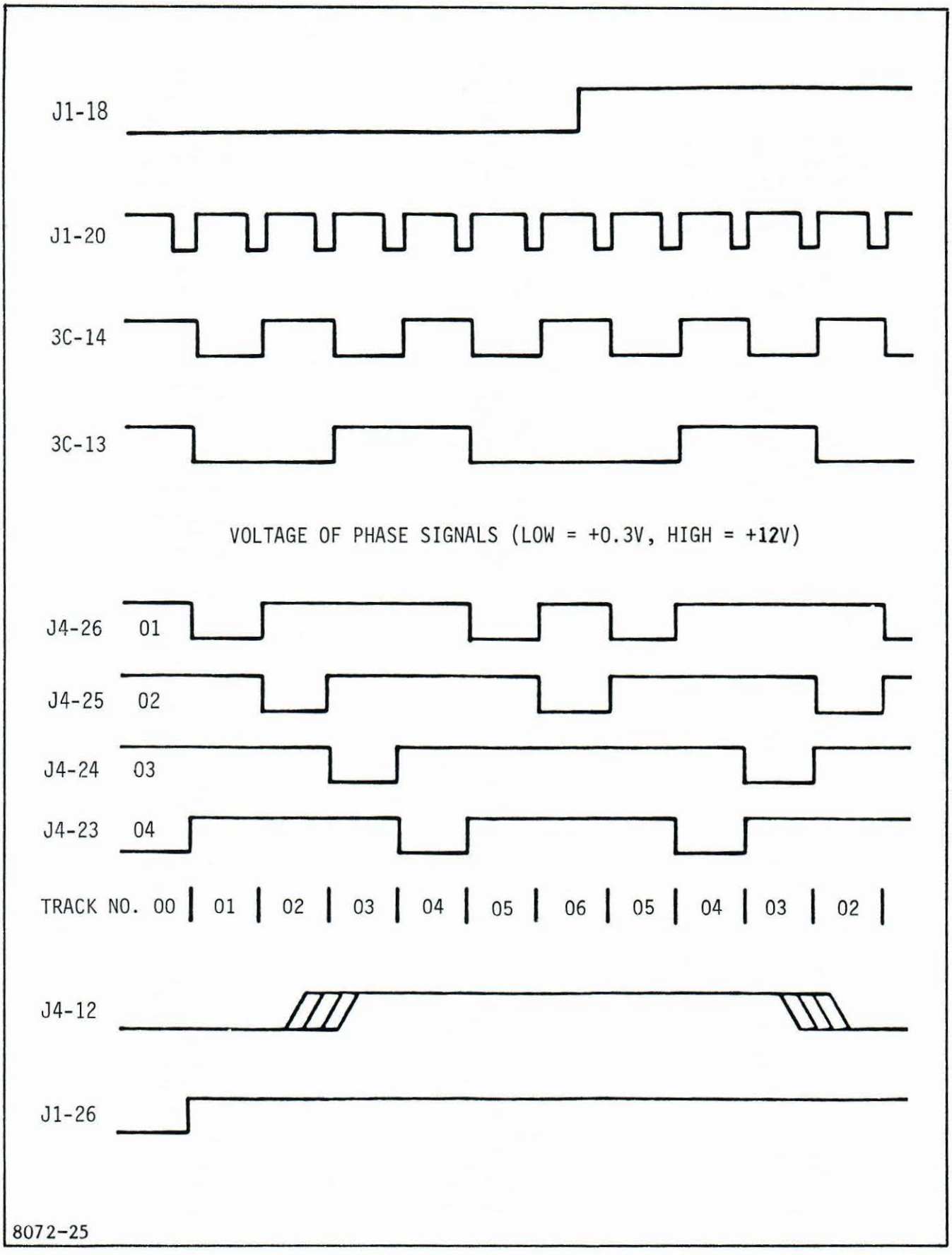


Figure 4-7. Stepper Motor Control Timing

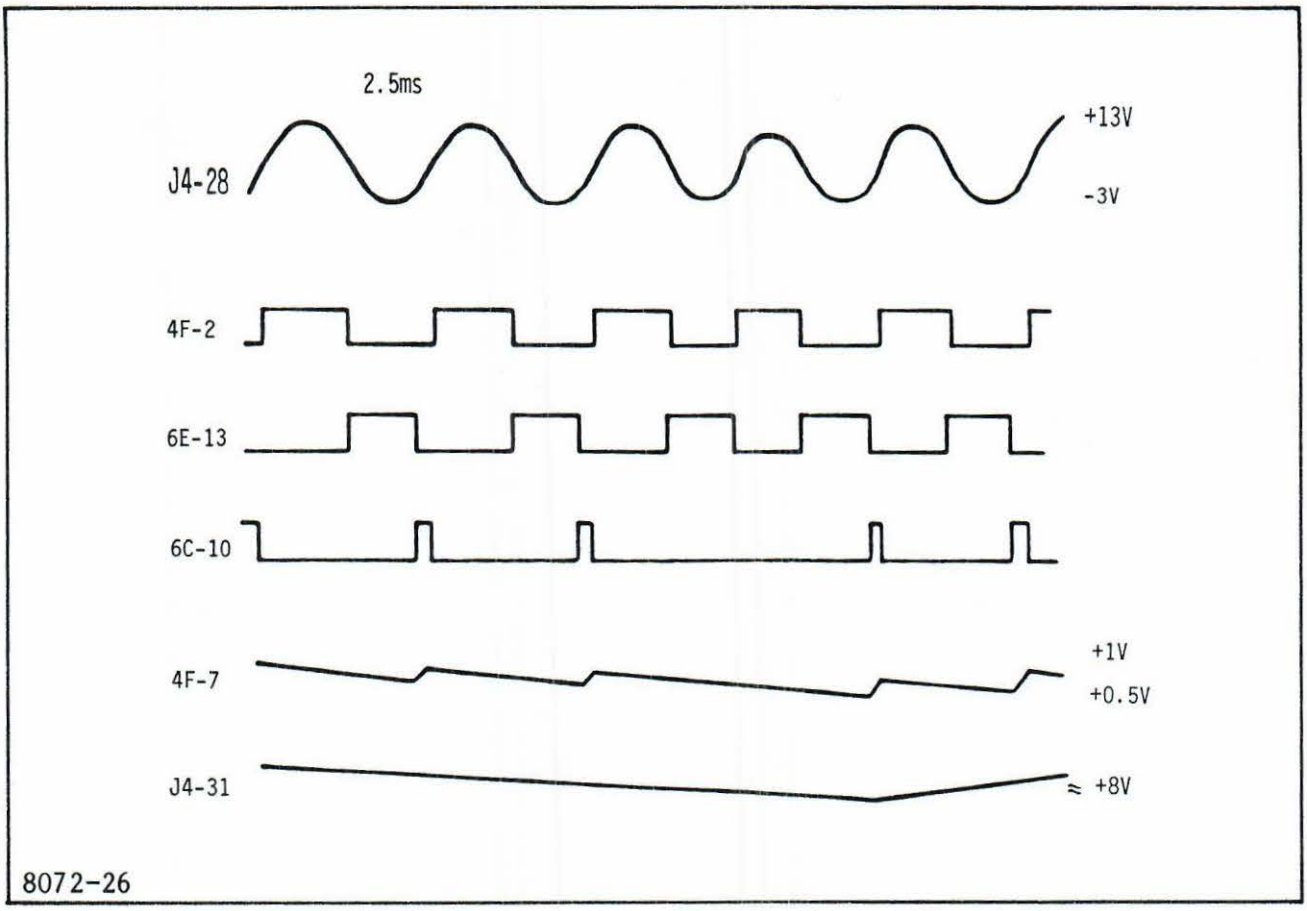


Figure 4-8. Motor Control Timing

4.6.8.5 Head Will Not Load

1. Check driver 5G pin 3 for a low level. If output is low, replace head load solenoid.

2. Double-check shunt 1G for proper programming.

4.6.8.6 Bad Index Output

1. Block index LED light path. If J4-B is a low level, replace index/load boss assembly.

2. Remove diskette and close door. Check J4-8 for a low level; if J4-8 is low proceed to step 5.

3. Check J4-6 for approximately 1.5 volts; if J4-6 is 0 volt or +5 volts, replace carrier.

4. If J4-6 is approximately 1.5 volts, replace index/load boss assembly.

5. Check for correct signal levels throughout index logic.

4.6.8.7 Bad Write Protect Output

1. Block write protect LED light path. If J4-16 is a low level, replace right hand guide/write protect assembly.

2. Unblock write protect LED light path. If J4-16 is a high level, replace right hand guide/write protect assembly.

3. Check for correct signal levels throughout write protect logic.

4.6.8.8 Activity Indicator Does Not Light

1. Check activity indicator logic for correct signal levels.

2. If signal levels are correct, replace activity indicator.

4.6.8.9 Read Errors - All Tracks

1. Verify that head is loaded by visually checking that head load pad (or upper head on Model 92) contacts diskette. If head is not loaded refer to paragraph 4.6.8.5.

2. Check compliance (refer to paragraph 4.5.1.8). If compliance is bad, replace load pad assembly and/or clean head.

3. Check read logic for proper signals as compared with timing diagram, figure 4-10.

4. On Model 91 drives, J1-32 must be high in order to read.

5. Check HD0 READ (or HD1 READ if checking read of top head on Model 92) for a low level.

6. With power removed from the PCBA, check CR4, CR5, Q1, and Q2 for proper readings.

7. Replace PCBA. If still no read signals from drive, replace head/carriage assembly.

4.6.8.10 Read Errors - Random Tracks

Replace drive motor.

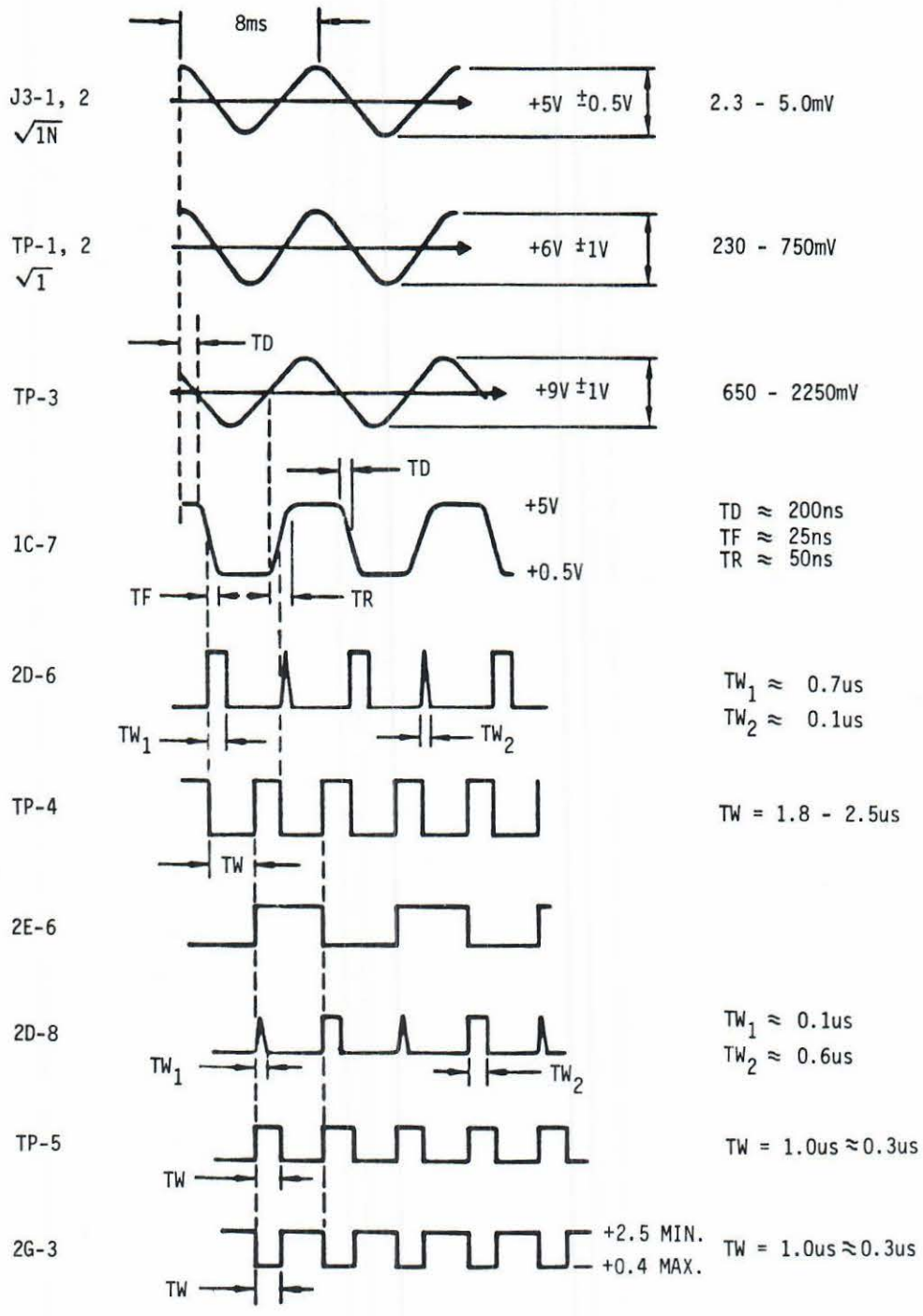


Figure 4-9. Read Timing

4.6.8.11 Read Errors - Inside Tracks

Verify that shield assembly is installed on carrier.

1. Check compliance (refer to paragraph 4.5.1.8). If compliance is bad, replace load pad assembly and/or clean head.

2. Check erase capability (refer to paragraph 4.5.1.9). If erase bad, refer to paragraph 4.6.8.14.

3. Check high frequency output (refer to paragraph 4.5.1.10). If output is bad, replace head/carriage assembly.

4. Replace amplifier integrated circuit chip 2A on PCBA.

4.6.8.12 Cannot Read Prewritten Data: Can Read Self-Written Data

1. Check radial track alignment (refer to paragraph 4.5.1.1).

2. Check index-to-data alignment (refer to paragraph 4.5.1.2).

4.6.8.13 Cannot Write Data

1. Check WRITE PROTECT output (refer to paragraph 4.6.8.7).

2. Check HD0 WRITE (or HD1 WRITE if top head on Model 92) for low level.

3. Check PCBA write circuits for correct signals per timing diagram, figure 4-11.

4.6.8.14 Erase Bad

1. If no decrease in amplitude is observed after the 15-second period outlined in paragraph 4.5.1.9, replace head/carriage assembly.

2. If amplitude decrease is less than 85%, replace load pad assembly and/or clean head.

4.6.8.15 Drive Speed Unstable

1. Check for bad spindle bearings by removing drive belt belt and slowly rotating spindle pulley manually. If spindle pulley rotates erratically, return drive to the factory to have spindle bearings replaced.

2. If spindle speed drifts slowly, replace capacitor C19 on the PCBA.

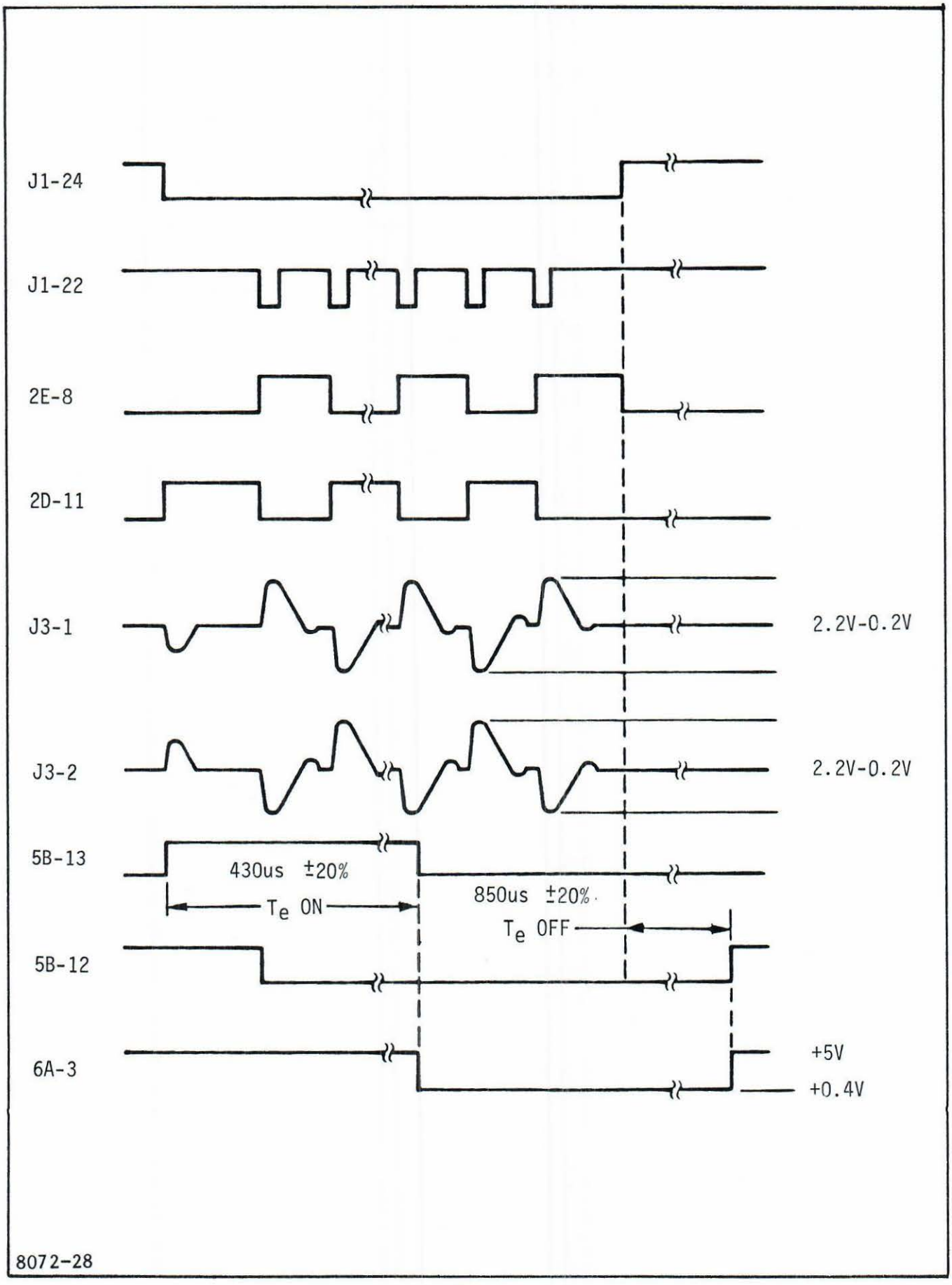


Figure 4-10. Write Timing

4.7 PERFORMANCE TESTS

If the unit under test performs all of the procedures properly, it is ready for use. If it fails, the test that fails and the condition of the failure will give an indication of the location of the fault. These tests are useful for checking that a unit is working after repair, or to determine the location of a fault if the service technician has not seen the fault condition.

The first group of procedures checks functions on the AVP board, including memory integrity, video attributes, character generation, display linearity, and the operation of the keyboard. The second group verifies the operation of the disk drives, disk drive control and the second processor and memories.

4.7.1 ODT Terminal Integrity and Confidence Tests

The integrity and confidence tests check ROM and RAM circuits by performing checksum tests on all memory locations. These tests are normally run automatically at power up or whenever FUNCTION and RESET are pressed together. To start the tests on the terminal manually, proceed as follows:

a. Press FUNCTION and LINE/LOCAL or REMOTE/LOCAL to set the terminal to local operation.

b. Press FUNCTION/TEST (PF8).

The ODT will immediately run the test once. If the test is successful, the prompt will be displayed and the unit is ready for a command.

If an error occurs, either a SYS ERR-RAM, ROM, or NVR message will appear in the status line or one of the following characters will appear in the first position of Status Line One:

- If a ROM error occurs, a " character will appear.
- If an NVR error occurs, a ! character will appear.
- If an error in Read/Write memory occurs, a $ character will appear.
- If an error occurs in both the ROM and NVR, a # character will appear.
- If errors occur in both the ROM and Read/Write memory, a & character will appear.
- If errors occur in both the NVR and Read/Write memory, a % character will appear.
- If errors occur in NVR, ROM and Read/Write memory, a ' character will appear.

4.7.2 Display Attribute Tests

The display attribute tests check display blinking, bold, reverse video, underscore, double wide and double high functions. These checks verify the operation of the Line Buffer and Character Generator circuits. Characters typed after the invoked attribute in each of the following steps should immediately assume the attribute. Refer to the Escape and Control Sequences Section of the appropriate User's Guide for video attribute operation.

NOTE

CAPS LOCK must be OFF to invoke the following attributes.

If the unit does not respond properly to programmatic control, control characters may be displayed on the screen by pressing FUNCTION/M. Control characters will be displayed and underscroed on the screen but will not be executed. The line may then be monitored and the fault diagnosed. Press FUNCTION/M again to exit the control character display mode. For HP compatible units, use FUNCTION/DISPLAY FUNCTIONS instead of FUNCTION/M.

To test the video attributes for the terminal, proceed as follows:

1. Press FUNCTION/LINE-LOCAL or FUNCTION/REMOTE-LOCAL for the Local Mode.

2. Press ESCAPE[5m (HP compatible: ESCAPE&dA) for blinking video and a type a string of characters.

3. Press ESCAPE[im for bold video (HP compatible: ESCAPE&dH for half intensity) and type a string of characters.

4. Press ESCAPE[7m (HP compatible: ESCAPE&dB) for reverse video and type a string of characters.

5. Press ESCAPE[4m (HP compatible: ESCAPE&dD) for underscore (underline) and type a string of characters. Each character appears with an underline as it is typed.

6. Press ESCAPE#6 (no HP equivalent) for double-wide video and type a string of characters.

7. Press ESCAPE#3 (no HP equivalent) for double high for the top half of displayed characters. Type a string of characters. Only the top half of each character will appear as it is typed.

8. Using the Cursor UP, DOWN, RIGHT and LEFT keys (indicated by the arrows) move the cursor down one line and press ESCAPE#4 (no HP equivalent) for double-wide for the bottom half of each typed character. The cursor will double in width and jump below the last character typed in step 7.

9. Move the cursor below the first character typed in step 7. Type the same character string entered in step 6. The bottom half of the character will appear on the screen.

10. Move the cursor to the beginning of the double high character line and press ESCAPE#5 (no HP equivalent) to reset the line to single high characters.

11. Move the cursor to the beginning of the line containing the remainder of the double-high characters and press ESCAPE#5 to reset the line to single-high characters.

4.7.3 Key Function Tests

The following tests verify the operation of keyboard dedicated function keys, and the selections of alternate character sets.

4.7.3.1 Tabstops

To check the setting and clearing of tabs, proceed as follows:

1. Press FUNCTION/LINE-LOCAL or FUNCTION/REMOTE-LOCAL to select Local Mode.

2. Press the TAB key several times. The cursor will advance incrementally to each tabstop set.

3. Press FUNCTION/CLEAR ALL TABS, then press TAB again. The cursor will advance to column 80 (or 132 if set).

4. Press RETURN to return the cursor to column 1. Advance the cursor with either the space bar or --). Press FUNCTION/SET-CLEAR TABS to set at arbitrary column positions.

5. Repeat step 2 to verify the tab positions set in step 4.

4.7.3.2 Status, Keyclick, and Margin Bell

To check the STATUS, KEYCLICK, and MARGIN BELL key functions, proceed as follows:

1. Press FUNCTION/STATUS several times. The Status Line should display the various status line types, then go blank, and continue in sequence as the key combination is pressed. On HP compatible units, the status line and PF key labels should be alternately displayed.

2. Press FUNCTION/KEYCLICK, then type a string of characters. If the Keyclick was on, it should now be off; if off, it should now be on. press the FUNCTION/KEYCLICK keys again to check the toggle action.

3. Move the cursor to the right side of the screen with the space bar or --). The Margin Bell, if on, will sound when the cursor is eight characters from the right margin.

4. Press FUNCTION/MARGIN BELL and repeat step 3 to check the Margin Bell toggle.

4.7.3.3 Auto Repeat and Scroll Rate

To check these features, do the following:

1. Press FUNCTION/AUTO REPEAT, then type a character and hold down the key. If Auto Repeat is on, the character will repeat until the key is released. If Auto Repeat is off, the character will appear once each time the key is pressed.

2. Press FUNCTION/AUTO REPEAT and repeat step 1 to check its toggle action.

3. Type characters in any form to fill a few lines on the display. Press FUNCTION/SCROL UP or FUNCTION/SCROL DOWN. The displayed text will scroll incrementally or smoothly, depending on the mode set.

4. Press FUNCTION/SCROLL RATE one time and repeat step 3 twice to check the toggle action between the other two scroll rates.

4.7.3.4 Screen, Column Width, Cursor, and Reset

To check reverse video, column width, and cursor, proceed as follows:

1. Press FUNCTION/SCREEN. The screen background should reverse from light to dark, or dark to light.

2. Type a character string, then press FUNCTION/80-132. The screen should immediately go blank.

3. Type another character string. The displayed characters will appear either larger or smaller than the string typed in step 2.

4. Press FUNCTION/80-132 again and type another character string to check the toggle action.

5. Press FUNCTION/CURSOR. The cursor should change between block style and underline.

6. Press FUNCTION/CURSOR again to check its toggle action.

7. Press FUNCTION/RESET. The bell should sound, and the screen will go blank.

4.7.4 Saving Set-Up Features

To check the operation of the NVR, which saves features when they are set up, proceed as follows:

1. Go to Set-Up mode (refer to appropriate section in User's Guide) and record the set-up parameters. Include all features that can be saved.

2. Arbitrarily change the parameters in step 1.

3. Pressing FUNCTION/S or FUNCTION/CONTROL/S (see note below) saves these changes. When WAIT is gone from the Status Line, compare the indicated parameters with those stored in step 2.

4. Change the parameters back, then SAVE. (see note below).

NOTE

Enter FUNCTION/S when testing ODT and enter FUNCTION/CONTROL/S when testing S/10 system.

4.7.5 Screen Linearity and Focus Test

These units contain a built-in pattern generator for checking and adjusting the display presentation. This generator fills the screen with E characters. To check display linearity and focus, proceed as follows:

1. Put the terminal into Local mode.

2. select 132-column mode.

3. Press ESCAPE#8 (ESCAPE#8 for the ODT and ESCAPE/SPACE BAR for S/10). The screen will immediately fill with Es.

4. Check the sharpness of the characters and the linearity (squareness) of the display.

5. Erase the display by either moving the cursor to the home position and pressing FUNCTION/EP or selecting the 80-column mode.

If the display requires adjustment, go to the adjustment procedure in paragraph 4.5.2. This concludes the integrity, keyboard and display tests.

4.7.6 S/10 Memory, EPROMs, and Disk Drive Tests

The S/10 system has display and keyboard characteristics similar to those for the Terminal. Those tests for the ODT Terminals are also applicable for testing the S/10. Additional tests are required to check the diskette drives, drive controller and the computer microprocessor and memory. To run the standard tests, load the S/10 with the SYSTEM disk supplied with the unit.

The alignment of the heads is checked using the VERIFICATION disk available for this test. This is a standard floppy diskette which has been formatted on a master disk drive. The head to track alignment is checked when this disk is Verified using the FORMAT program. Do not format this disk or the original tracks and sectors will be erased.

When the S/10 is powered up or the FUNCTION/RESTART key combination is pressed, all memories are cleared, and the operating system is loaded from the diskette to the computer RAM. This is a process which requires that all parts of the system function together. When the unit is running under CP/M, the EPROM, RAM, controller and disk drive, as well as terminal and display functions, have been verified. If the power up procedure does not work, refer to the Troubleshooting Chart, table 4-1. There are two other levels of reset which can be used to reset the unit: a warm reset, where the data buffers are cleared, and a terminal reset in which only those buffers related to the display are cleared.

If any of these tests cannot be completed, refer to the Troubleshooting Chart, table 4-1 in this manual.

4.7.6.1 Power Up Test

To start the tests manually, proceed as follows:

1. Check that no diskettes are loaded.
2. Switch power ON.
3. Load the SYSTEM diskette into the top drive.
4. Display Status Line One by pressing the FUNCTION/STATUS key combination until it appears. Status Line One is the line in which the rightmost field is Sel=.

The S/10 runs the test once, and responds with A>. If the test is completed successfully, go to paragraph 4.7.6.2 for the next test. The error message appears in the first position of Status Line One as follows:

- o If a ROM error occurs, a " character will appear.
- o If an NVR error occurs, a ! character will appear.
- o If an error in Read/Write memory occurs, a $ character will appear.
- o If an error occurs in both the ROM and NVR, a # character will appear.
- o If errors occur in both the ROM and Read/Write memory, a & character will appear.
- o If errors occur in both the NVR and Read/Write memory, a % character will appear.
- o If errors occur in NVR, ROM and Read/Write memory, a ' character will appear.

In all cases, the ROM and RAM memories referred to here are those on the Advanced Video Processor board. See the Troubleshooting Chart for the required action.

4.7.6.2 Verifying Data from the Diskette

To verify data read from a diskette, proceed as follows:

1. Insert the CP/M diskette (with the FORMAT program) in the upper drive.
2. Insert the disk to be verified in the lower drive.
3. Type FORMAT and press RETURN to call up the FORMAT program.
4. Follow screen instructions, and verify the data on the diskette in the lower drive. Refer to the appropriate Operator's Reference Guide for detailed instructions on using this program.

WARNING

Select VERIFY for this test, otherwise the data on the diskette will be erased. Always keep backup copies of all diskettes.

At the conclusion of the test, there should be no error messages. The display indicates how the test is terminated. For an successful test, there will be an error message. If errors occur, refer to paragraph 4.7.1. If the test is completed successfully, go to paragraph 4.7.6.3.

4.7.6.3 Check the Other Disk Drive

To check the performance of the other disk drive, proceed as follows:

1. Remove both diskettes from the drives.
2. Turn off power to the unit.
3. Pause for 5 seconds, then turn the power back on.
4. Repeat the steps in paragraph 4.7.6.1, but loading the SYSTEM diskette into the lower drive.
5. Repeat the steps in paragraph 4.7.6.2 but loading the VERIFICATION diskette into the upper drive.

4.7.7 S/10 Display Attribute Tests

The display attribute tests for the S/10 are identical to those of the ODT Terminal. Refer to paragraph 4.7.2 for the test procedures.

4.7.8 S/10 Key Function Tests

Procedures for checking the operation of the tabstops, status, keyclick, margin bell, auto repeat, screen and saving setup features are given in paragraph 4.7.3 of this section.

4.7.9 S/10 Screen Linearity and Focus Test

All display components are identical for both the ODT and S/10. Refer to paragraph 4.7.5 for these procedures.

4.7.10 Testing Serial Ports

This test checks the operation of the two serial ports. The first test verifies that the ports are both working, and if the test is successful, is all that is required. If the test indicates a fault, continue to the second test. The S/10 can be returned to service by replacing board #1. The second test determines whether port #1 or port #2 is faulty, and whether it is the USART or baud rate generator. This aids in troubleshooting the board.

a. The Serial Port Test

To test the serial input/output (I/O) ports, proceed as follows:

1. Connect an RS232 cable from port #1 to port #2.

2. Enter PORTEST.

3. Enter PF1. This conducts a test of the ports, and indicates if they are operating correctly.

4. If the test indicates no fault, press PF7 to reboot BBM/CPM. If a fault condition is indicated, go to the test in step 2.

b. Identifying a faulty Port

To identify a faulty I/O port, proceed as follows:

1. Connect a terminal or host computer to the port.

2. Press PF5.

3. Enter data at the keyboard; check that data displayed follows the entered data.

4. If the test is good, check the other port. Note the error messages that occur.

5. Press PF7 to reboot CP/M.

SECTION V

REMOVAL/REPLACEMENT

5.1 INTRODUCTION

The following paragraphs provide detailed procedures for replacing and adjusting the major assemblies.

5.2 REPLACING THE AVP AND AFC BOARDS (BOARD #1 AND #2)

To replace either of these boards, proceed as follows:

CAUTION

Do not remove these boards when power is applied to the unit.

1. Turn the unit OFF.
2. Unplug any other equipment connected to the unit.
3. Lower the keyboard, and rotate the cabinet cover latch fully clockwise.
4. Using a flat, non-metal tool such as a plastic letter opener, open the top cover.
5. The faulty board may now be lifted out. The cables must be detached from the Controller board prior to lifting it out of the case. See figure 1-2 for board identification.
6. To install the replacement board, reverse steps 3, 4 and 5.

5.3 POWER SUPPLY/REGULATOR REPLACEMENT

NOTE

The correct power supply for the ODT Terminal or System S/10 must be installed. See the parts listing for part numbers.

To replace the Power Supply/Regulator assembly, proceed as follows:

1. Turn the unit OFF.

2. Lower the keyboard, and rotate the cabinet cover latch fully clockwise.

3. Using a flat, non-metal tool such as a plastic letter opener, open the top cover.

4. The faulty assembly may now be lifted out. See figure 1-2 for the assembly location.

5. Install the replacement assembly in the reverse order of steps 2 through 4.

6. Turn the unit ON.

7. Connect a DVM across the test point on the AVP board for +5VDC and ground, see figure 4-3.

8. Set the adjustment on the Power Supply to between +5.00 and +5.03VDC, see figure 4-3. There is no minus tolerance on this adjustment.

9. Disconnect the DVM.

WARNING

Hazardous voltages are exposed in the cabinet. Be extremely careful when servicing the power supply or any area where power terminals are exposed.

An implosion danger always exists with CRTs. Be careful when working around the neck of the CRT.

10. Return the unit to normal operation.

5.4 VIDEO ELECTRONICS ASSEMBLY REPLACEMENT

To replace the Video Electronics assembly, proceed as follows:

1. Turn the unit OFF.

2. Discharge the high voltage anode by sliding a screwdriver grounded to the chassis under the HV cap on the tube.

3. Disconnect the HORIZONTAL YOKE, VERTICAL YOKE and flyback transformer cable connectors from the Video assembly (see figures 1-2 and 5-1).

4. Disconnect P5 from J5 on the Video electornics assembly.

WARNING

Hazardous voltages are exposed in the cabinet.
Use extreme caution when servicing any area
where power terminals are exposed.

5. Unplug the CRT connector from the CRT neck (see figure 5-2).

WARNING

An implosion danger always exists with CRTs.
Be careful when working around the neck of
the CRT.

6. Disconnect the ground lead from the CRT grounding clip.

7. Using needle nose pliers, pinch the mounting clip locks and lift the Video assembly off the mounting clips. Remove from the unit.

8. Install the replacement Video electronics assembly in the reverse order of steps 3 through 7.

9. Adjust the video display in accordance with paragaph 4.5.2.

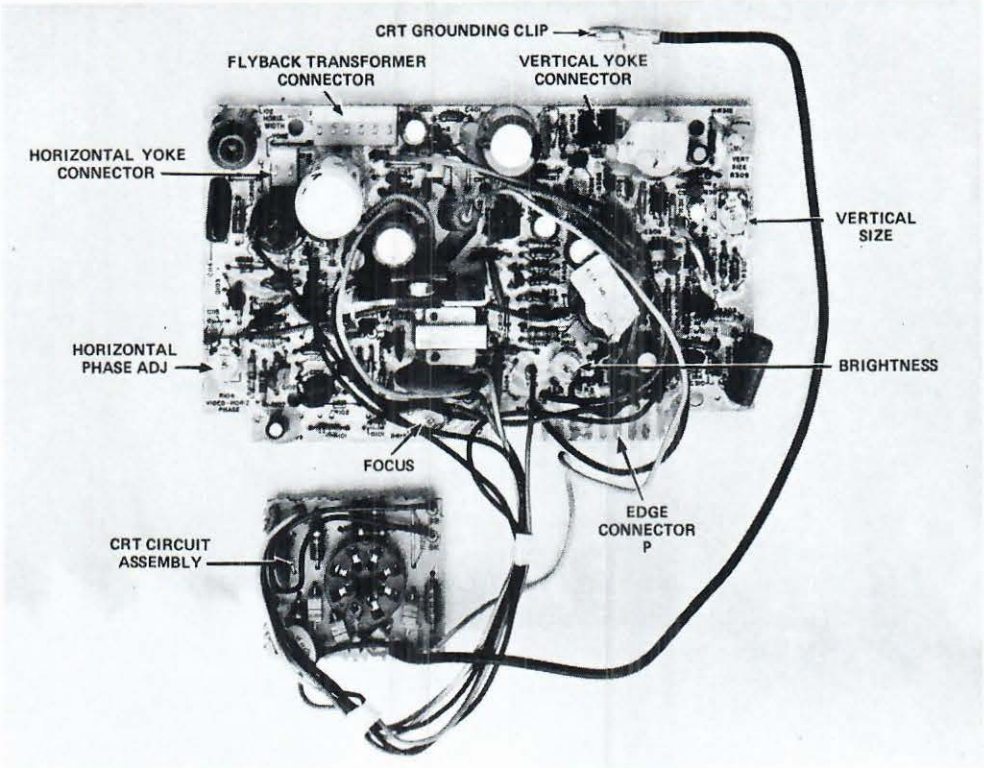


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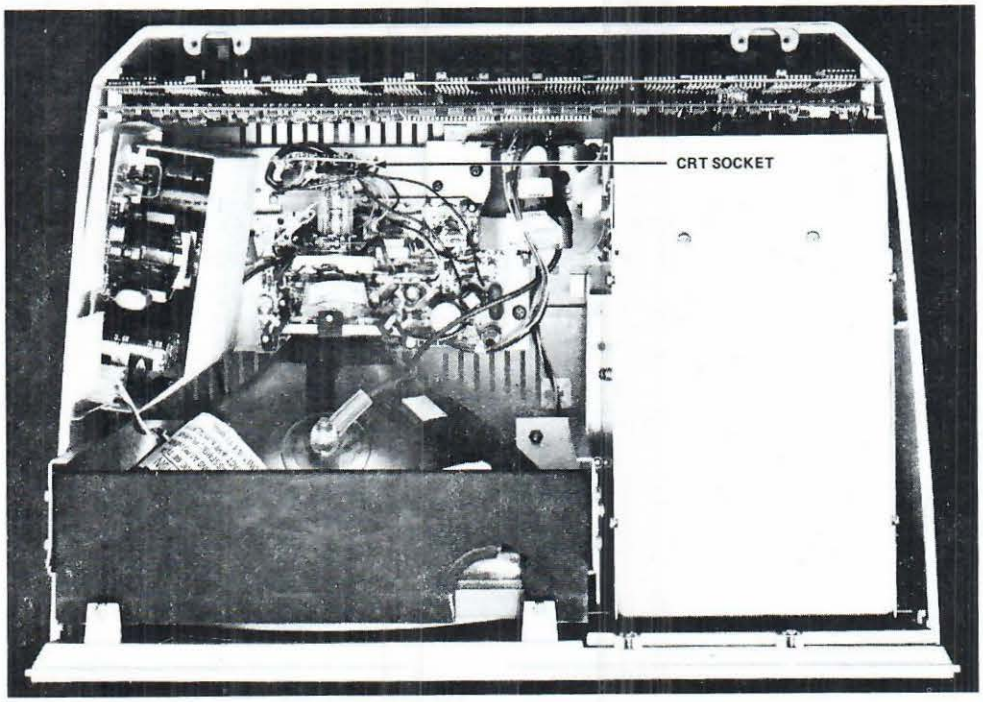
Figure 5-1. Video Electronics Assembly



8072-30

Figure 5-2. CRT Connector

5.5 FLYBACK TRANSFORMER REPLACEMENT

To replace the flyback transformer, proceed as follows:

WARNING

When the power is off, dangerously high voltages may be retained by the CRT anode. To avoid injury, remove the AVP and Controller boards, then discharge the CRT anode to ground before unclipping the high voltage lead.

1. Turn the unit OFF.
2. Pinch the high voltage lead anode clip perpendicular to the lead (see figure 5-3) to remove it from the CRT.
3. Remove connector with high voltage drive leads from video assembly.
4. Lift the transformer from the Motherboard.
5. Install the replacement flyback transformer in the reverse order of steps 2 through 4, and return to normal operation.

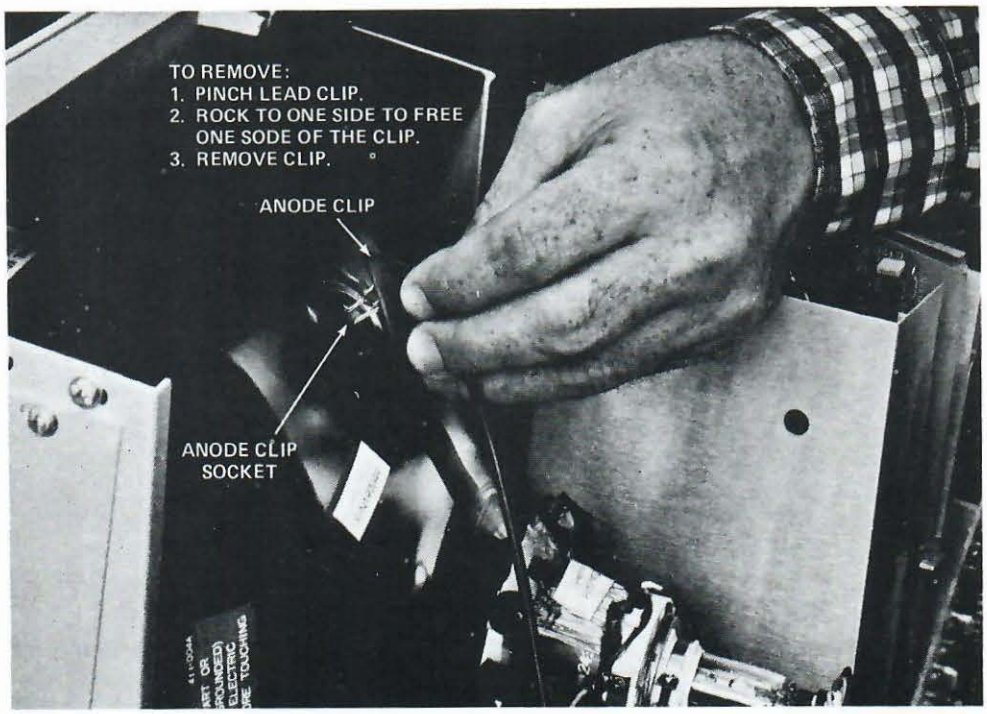


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Figure 5-3. Removing the CRT High Voltage Anode Lead

5.6 POWER SOCKET AND SWITCH ASSEMBLY REPLACEMENT

To replace the primary power socket and switch assembly, proceed as follows:

1. Turn the unit OFF and disconnect the power cord.
2. Turn the unit upside-down and remove the 2 screws securing the assembly to the cabinet.
3. Tag the power leads to the on/off switch, then remove it.
4. Unsolder the leads to the line filter.
5. Disconnect the ground lead to the line filter.
6. Disconnect the wires to the keyboard cable jack.
7. Remove the assembly.
8. Install the replacement assembly in the reverse order of steps 2 through 7.
9. Reconnect the power cable and return the unit to normal operation.

5.7 CRT REPLACEMENT

The unit must be disassembled to replace the CRT.

WARNING

An implosion hazard always exists with CRTs. Do not handle the CRT by its neck. Be extremely careful when working around the CRT neck.

The coating on the inside of CRTs is poisonous. If the CRT breaks, wear heavy rubber gloves or use tongs (or a similar tool) to pick up the broken fragments.

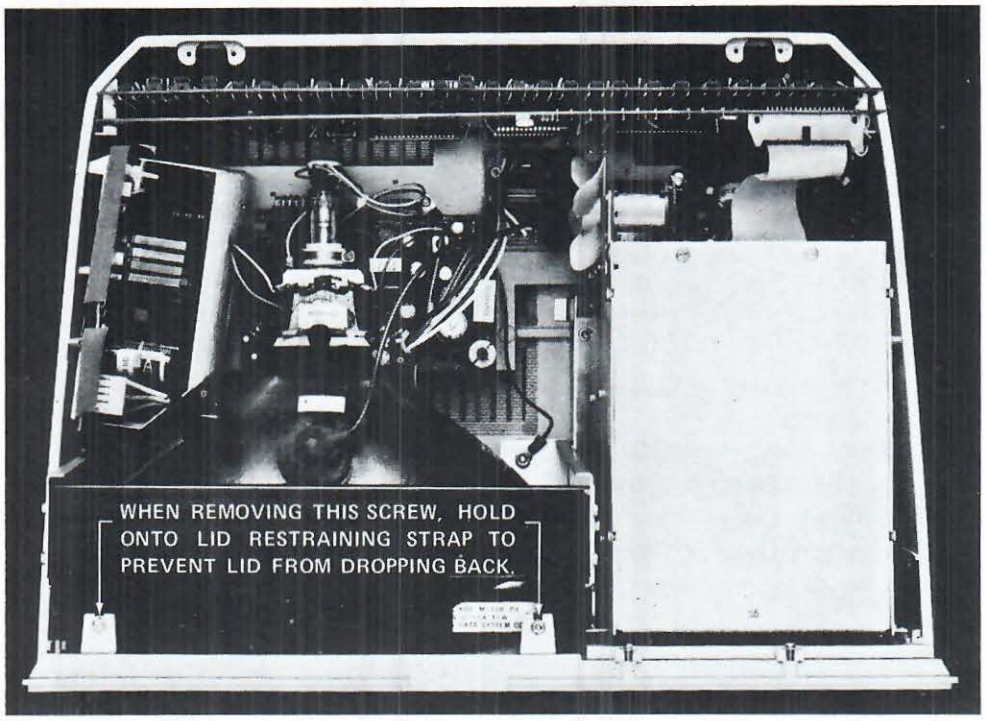
To remove and reinstall the CRT, proceed as follows:

1. Turn the unit OFF.
2. Remove the AVP and Controller boards (refer to paragraph 5.2).
3. Remove the Power Supply (refer to paragraph 5.3).
4. Unplug the CRT connector from the CRT neck. (see figure 5-2).

WARNING

When the power is off, dangerous potentials may be retained by the CRT anode. To avoid injury, remove the AVP and Controller boards, then discharge the CRT anode to ground before unclipping the high voltage lead.

5. Pinch the high voltage lead anode clip perpendicular to the lead (see figure 5-3) to remove the clip from the CRT.
6. Disconnect the HORIZONTAL YOKE and VERTICAL YOKE leads from the Video board.
7. Remove the two screws securing the primary power connector and switch assembly (see figure 2-1) and cut the cable harness tie wraps if necessary.
8. Secure the unit on its side and remove the four screws that secure the chassis to the bottom of the cabinet.
9. Set the unit back on its base and remove the two screws that secure the chassis to the top of the cabinet (see figure 5-4).
10. Slide the chassis to the rear approximately 1/2 inch to disengage the rear of the chassis. Gently lift the chassis from the cabinet and set it on its base on a clear, flat work area.
11. Remove the two screws securing the bottom two lugs of the CRT frame to the chassis.
12. While supporting the CRT face with one hand, remove the two screws securing the top two lugs of the CRT frame to the chassis.
13. Remove the CRT from the chassis and place in the replacement CRT's shipping container. Dispose of the CRT in a safe manner.



8072-32

Figure 5-4. Chassis Top Securing Screws

14. To install the replacement CRT, proceed in the reverse order of steps 2 through 13. Install the new tube with the anode socket UP! Also ensure that the aquadag grounding clip is reinstalled when the top right CRT frame lug screw is installed.

NOTE

Do not tighten the CRT frame lug screws until the last one is in place.

5.8 KEYBOARD REPLACEMENT

The keyboard consists of the keyboard cabinet, the keyboard assembly (a Field Replaceable Unit), and a +5 VDC regulator. To replace the keyboard assembly, proceed as follows:

1. Turn the unit OFF.
2. Remove the keyboard cover using a non-metalic, flat blade instrument (such as a plastic letter opener) to lift the front edge.
3. Remove the 4 screws holding the keyboard in its cabinet.
4. Disconnect the keyboard cord from the keyboard.

5. Remove the keyboard.

6. To install a replacement keyboard, reverse steps 2 through 5.

7. Return the unit to normal operation.

5.9 KEYBOARD HINGE REPLACEMENT

If the keyboard hinges need replacing, perform steps 1 and 2; if the right keyboard hinge on the terminal cabinet needs replacing, perform steps 3 through 6; if the left keyboard hinge on the terminal cabinet needs replacing, perform steps 7 through 11. To replace damaged keyboard hinges, turn off the unit and proceed as follows:

Keyboard Hinges:

1. Remove the keyboard cover.

2. Remove the two screws securing the hinges to the keyboard cabinet and install the replacement hinges.

Right Cabinet Hinge:

3. (S/10 only) remove the disk drive assembly as described in paragraph 5.11.

4. Remove the two screws securing the right keyboard hinge to the terminal cabinet.

5. Install the replacement hinge.

6. (S/10 only) reinstall the disk drive assembly as described in paragraph 5.11.

Left Cabinet Hinge:

7. Remove the CRT assembly as described in paragraph 5.7, steps 7 through 10.

8. Remove the two screws securing the left keyboard hinge to the cabinet.

9. Install the replacement hinge.

10. Reinstall the CRT assembly in the reverse order of paragraph 5.7, steps 7 through 10. Replace any cut tie wraps.

11. Return the unit to normal operation.

5.10 SPEAKER REPLACEMENT

To replace the keyclick/bell speaker (see figure 1-2) proceed as follows:

1. Turn the unit OFF.
2. Using a flat, non-metal tool such as a plastic letter opener, raise the cabinet cover. Remove the AVP board, and the Controller board.
3. (S/10 only) remove the disk drive assembly as described in paragraph 5.11.
4. Unsolder the speaker leads.
5. Remove the 2 screws securing the speaker to the Motherboard.
6. Install the new speaker in the reverse order of steps 4 and 5.
7. (S/10 only) reinstall the disk drive assembly as described in paragraph 5.11.
8. Reinstall the AVP board. Reinstall the controller board.
9. Return the unit to normal operation.

5.11 DISK DRIVE REPLACEMENT (S/10 ONLY)

To replace a malfunctioning disk drive, proceed as follows:

1. Trun the unit OFF and remove all external cables.
2. Using a flat, non-metal tool, open the cabinet.
3. Remove the AVP board and the Controller board.
4. Disconnect the ribbon connector and disk drive power cable.
5. Using a long shank screwdriver, remove the disk drive groundwire from the Motherboard grounding lug.
6. Disconnect the power connection at the power supply to the disk drive, and cut the cable ties on the Motherboard and flyback transformer shield.
7. Turn the unit onto its side on a soft surface and remove the four drive unit mounting screws (see figure 5-5).
8. Place the unit into its normal position and remove the two front panel screws (see figure 5-6).

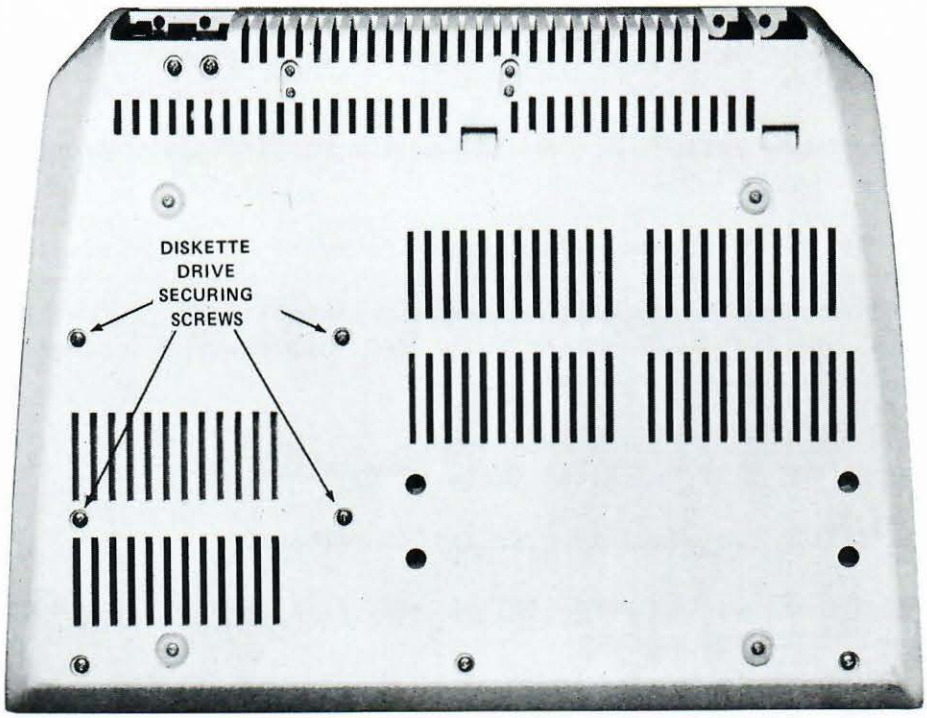


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Figure 5-5. Drive Securing Screws (S/10 Only)

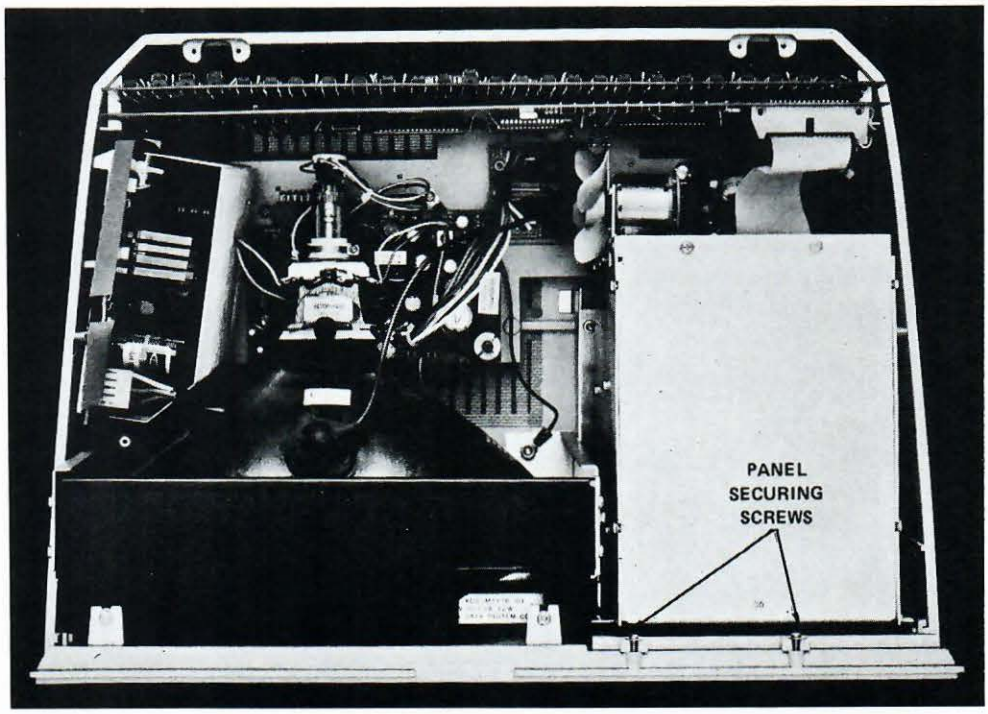

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Figure 5-6. Front Panel Securing Screws (S/10 Only)

9. Carefully lift the drive assembly back and out of the cabinet.

10. Remove the four (4) screws securing the front panel to the drive assembly.

11. Remove the screws in the side of the casting that secure the drives (see figure 7-3).

12. Slide the drives out through the front of the casting.

To install the drives in the cabinet, reverse this procedure. After the units are installed, check the alignment of the disk drive units as described in Section IV of this manual.

5.12 REPLACING THE DISK DRIVE FAN (S/10 ONLY)

To replace a faulty fan assembly, proceed as follows:

1. Using a flat, non-metal object such as a plastic letter opener, raise the top of the cabinet.

2. Cut the plastic tie that fastens the fan to the drive unit and unplug the fan cable.

To install a new fan, reverse the above procedure.

5.13 DISK DRIVE ASSEMBLY (S/10 ONLY)

The following material gives sequential instructions for removing and replacing major components of the disk drive. Table 5-1 lists the removal/replacement procedures contained in this section. Figures 5-7 and 5-8 are top and bottom views of the disk drive that illustrate the components for which replacement instructions are given. The appropriate paragraph should be referenced when performing any of these procedures. An exploded view of the disk drive is illustrated in Section VII and should be used only as a reference to familiarize yourself with the arrangement of the assemblies. Table 5-2 references assemblies that may need to be adjusted when major components are removed/replaced.

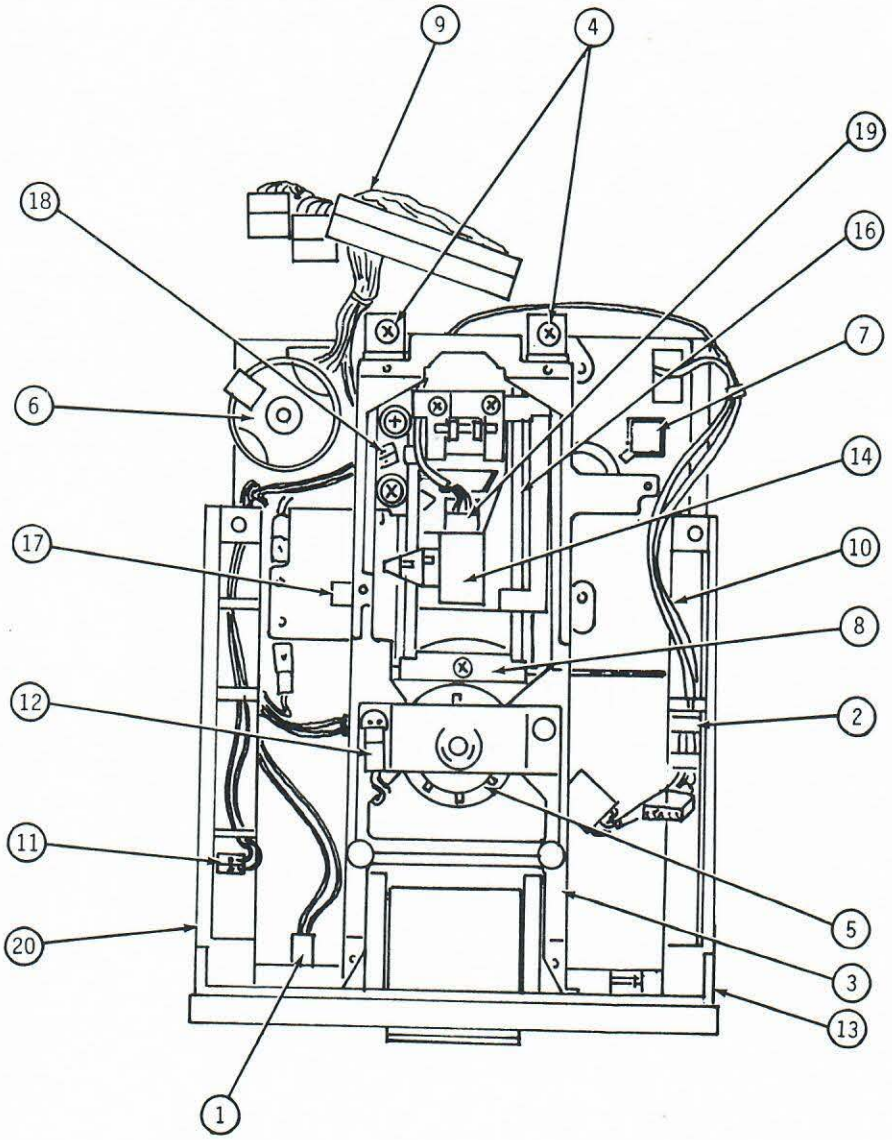

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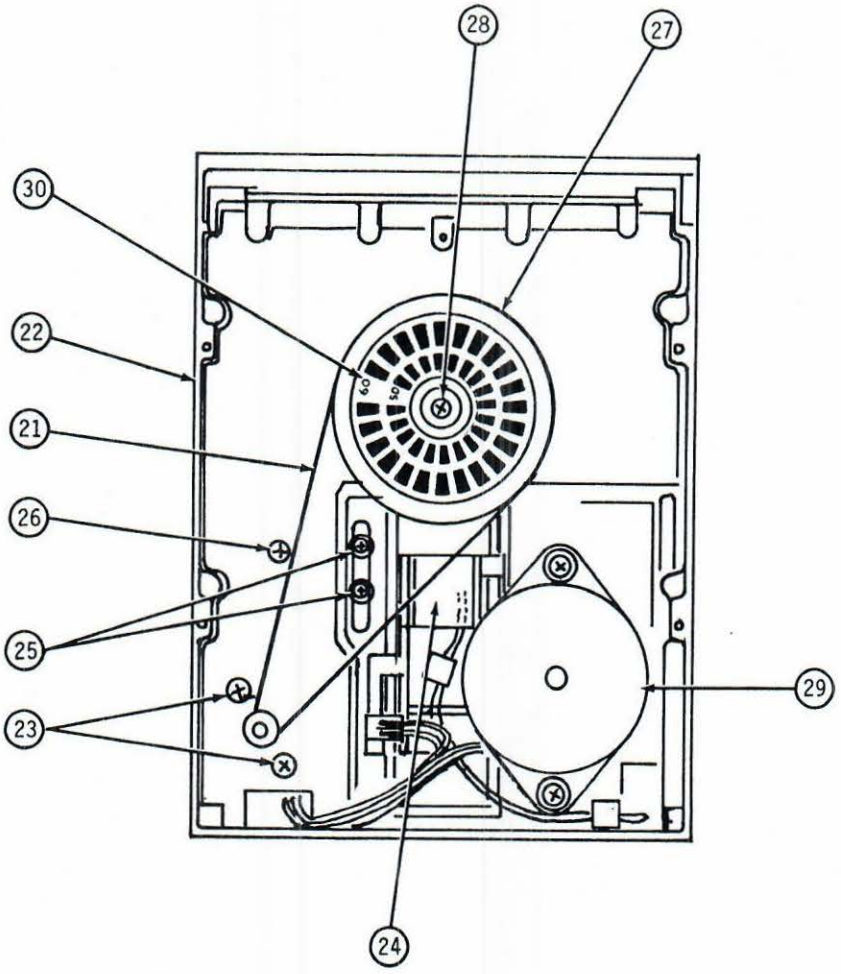
Figure 5-7. Disk Drive, Top View



8072-36

Figure 5-8. Disk Drive, Bottom View

Table 5-1. Removal/Replacement Procedures

PROCEDURE	PARAGRAPH
Printed Circuit Board Assembly (PCBA)	5.13.1
Shield Assembly	5.13.2
Right-Hand Guide/Write Protect Assembly	5.13.3
Left-Hand Guide Assembly	5.13.4
Front Panel Bezel and Activity LED	5.13.5
Cone Assembly	5.13.8
Carrier Assembly	5.13.9
Index/Load Boss Assembly	5.13.11
Solenoid	5.13.12
Drive Motor	5.13.13
Track 00 Sensor	5.13.14
Door Button Assembly (91/92 only)	5.13.15
Stepper Band	5.13.16
Stepper Motor	5.13.17
Head/Carriage Assembly	5.13.18
Spindle, Bearings and Pulley	5.13.19
Head Load Pad Assembly	5.13.20
Harness Assembly	5.13.21

Table 5-2. Removal/Replacement Adjustment Check List

ASSEMBLY	CHECK OR ADJUSTMENT	PARAGRAPH
Head/Carriage	Radial-track alignment Track 00 sensor alignment Track 00 setscrew adjustment Compliance	4.5.1.1 4.5.1.3 4.5.1.5 4.5.1.9
Stepper Motor	Radial-track alignment	4.5.1.1
Track 00 Sensor	Track 00 sensor alignment	4.5.1.3
Index/Load Boss	Index-to-data alignment	4.5.1.2
Carrier	Index-to-data alignment Ejector (91/92 only)	4.5.1.2
Printed Circuit	Drive motor speed	4.5.1.4
Board (PCB)	Index-to-data alignment	4.5.1.2
Drive motor	Drive motor speed Drive belt	4.5.1.4
Spindle Pulley	Drive motor speed Drive belt	4.5.1.6
Head Load Pad	Compliance	4.5.1.9

5.13.1 Printed Circuit Board Assembly (PCBA)

To remove the printed circuit board (PCBA) proceed as follows:

1. Remove the I/O connector and DC power connector.
2. Remove screws (2) at each side of PCBA.
3. Pull PCBA slightly to the rear of the disk drive.
4. Remove head connector(s) below and at left front edge of PCBA. Grip the connector(s), not the cables when removing.
5. Remove connectors P4-1, P4-2, and P4-3 at right rear of PCBA.
6. Slide PCBA out the rear of the disk drive.

To replace the PCBA, perform the preceding steps 1 through 6 in the reverse order.

5.13.2 Shield Assembly

To remove the shield assembly located over the head/carriage assembly, proceed as follows:

1. The shield snaps over the carrier assembly; grip the left side, press down on the left-center of the shield, and lift the left side up. This will unsnap the shield from the left side of the carrier assembly.

2. Lift the shield to the right and up from the disk drive.

To replace the shield, perform the preceding steps 1 through 2 in the reverse order.

CAUTION

Be sure not to pinch the index LED wires under the right side of the carrier and the shield when installing.

5.13.3 Right-Hand Guide/Write Protect Assembly

The write protect sensor is an integral part of the right-hand guide. To remove this assembly, proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).

2. Remove screws (2) holding guide to the disk frame at the bottom of the guide.

3. Remove flat head, countersunk screw at top front of guide holding guide to bezel.

4. The guide is now free of the drive assembly.

5. Unplug the two female connectors from the write protect photo transistor and LED.

6. Remove the wires from the cable clamp. The guide/write protect assembly is now free of the drive assembly.

To replace the right-hand guide assembly, perform the preceding steps 1 through 6 in the reverse order. Be sure that:

a. The windows in the female connectors both face away from the guide when installed.

b. Wires to the write protect LED are routed through the cable clamp on the guide.

5.13.4 Left-Hand Guide Assembly

To remove the left-hand guide assembly, proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).
2. Remove screws (2) holding guide to the drive chassis at the bottom of the guide.
3. Remove flat head, countersunk screw at top front of guide holding guide to front panel bezel.
4. Remove head cable(s) from cable clamps. Guide is now free of drive assembly.

To replace the left-hand guide assembly, perform the preceding steps 1 through 4 in the reverse order.

5.13.5 Front Panel Bezel and Activity LED

To replace the activity indicator it is necessary to remove the bezel. To remove the bezel proceed as follows. Figure 5-9 shows the activity indicator mounting hardware:

1. Remove four (4) flat head, countersunk screws holding bezel to guides and drive chassis.
2. Open door to free bezel from door/carrier assembly.
3. Pull bezel forward slightly and remove female connector from activity LED. Bezel is now free of the drive assembly.

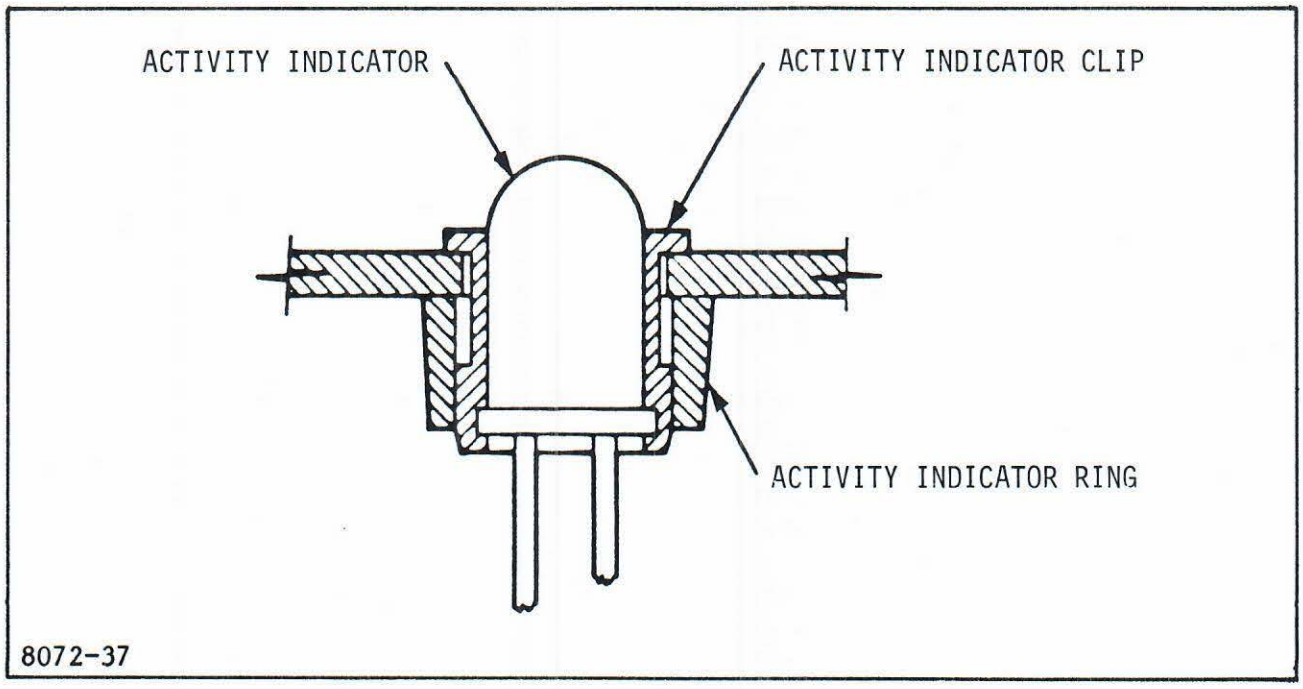


Figure 5-9. Activity Indicator Assembly

5.13.6 Activity LED Removal

To replace the activity LED, proceed as follows:

1. Remove bezel (refer to paragraph 5.13.5).
2. Loosen activity indicator ring around activity indicator clip and pry off.
3. From the font of the bezel, press LED out of the holder. This removes the LED.

5.13.7 Activity LED Replacement

To install the activity LED, proceed as follows:

1. Perform the steps in paragraph 5.13.6.
2. Press LED into clip in bezel from rear of bezel until it snaps in.
3. Hold LED clip with fingers and fit ring over rear part of clip. Press ring until it is flush against bezel.
4. Fit female connector over LED leads with green wire connected to longest LED lead.
5. Install bezel to drive chassis and guide assemblies (refer to paragraph 5.13.5).

5.13.8 Cone Assembly

The cone assembly fits within the drive spindle assembly. To remove this assembly, proceed as follows:

1. Be sure the door is closed.
2. Remove the snap ring and shims from the top of the carrier assembly.
3. Open door.
4. Cone will remain seated in spindle hub and can be lifted out of the drive assembly.

NOTE

Be sure to keep track of the number of shims between snap ring and carrier. The same shims must be replaced during installation.

To replace the cone assembly, perform the preceding steps in the reverse order.

NOTE

Be sure that the replacement cone has a shim and then a spring on the shaft of the cone before replacing it in the spindle hub.

5.13.9 Carrier Assembly

The carrier assembly lifts the cone from the spindle and the upper arm from the disk media when the door is opened. To remove this assembly, proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).
2. Remove shield assembly (refer to paragraph 5.13.2).
3. Remove cone assembly (refer to paragraph 5.13.8).
4. Remove screws (2) from rear of carrier holding carrier to drive chassis mounting posts.
5. Cut tie wraps holding index LED wires to carrier.
6. Remove index LED female connector.
7. 915/925 Only: Remove screws (2) attaching bezel to RH & LH guides and loosen screws (2) attaching bezel to chassis.

   91/92 Only: Remove screws (2) attaching carrier assembly to front door.
8. Open front door.
9. 915/925 Only: Swing top of bezel forward allowing door pins to slip free of bezel door slots.
10. The carrier is now free.

CAUTION

Do not lift the carrier straight up. The upper step of the upper head arm rests on top of the carrier assembly. Lifting carriage straight up may damage the head assembly.

Slide the carrier to the right to clear the head assembly upper arm, and lift out of the unit.

5.13.10 Carrier/Index LED

The index LED is part of the carrier assembly. The carrier assembly must be replaced to replace the index LED. To install this assembly, perform the following steps in the order listed:

1. Install carrier assembly by performing in reverse the procedures called out in paragraph 5.13.9, steps 1 through 10.
2. Install screws (2) in rear of carrier assembly loosely.
3. Install cone assembly (refer to paragraph 5.13.8).
4. Close door.
5. Center door in front opening of bezel.
6. Tighten rear carrier screws.
7. Install index LED female connector with connector windows down.
8. Tie wrap index connector wires to the carrier assembly at front and rear.
9. Perform any adjustment called out in table 5-2.

5.13.11 Index/Load BOSS

To remove the index/load boss assembly, proceed as follows:

1. Remove PCBA (refer to paragraph 5.13.1).
2. Remove shield assembly (refer to paragraph 5.13.2).
3. Remove index photo transistor female connector at front of boss assembly; pull to right side.
4. Place drive on its left size.
5. Remove the screws (2) in the adjustment slot in the recessed area in the base of the drive chassis.
6. Lift boss assembly up and out of the drive assembly.

To replace the index/load boss assembly, proceed as follows:

1. Place drive on its left side.
2. Install index/load boss assembly with LED toward front of drive.
3. Install screws loosely in the adjustment slot in the recessed area in the base of the disk drive chassis.

4. Install index photo transistor connector with windows toward drive chassis.

5. Perform any adjustments called out in table 5-2.

5.13.12 Solenoid

To remove the solenoid, proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).

2. Remove the right-hand guide (refer to paragraph 5.13.3).

3. Unsolder two leads from the solenoid. Note that older drives may have the leads attached to the solenoid with spade lugs.

4. Turn the drive on its side and remove the solenoid mounting screw (1) from bottom of drive chassis.

5. Solenoid is now free.

CAUTION

Be careful not to lift solenoid load arm straight up so that it bends upper arm assembly past its normal unloaded position.

6. Tilt solenoid and lift to the side and up out of the drive chassis.

To replace the solenoid perform the preceding steps in the reverse order, be sure that:

1. The bottom part of the load arm of the solenoid is beneath the index/load boss.

2. The top part of the load arm is beneath the top step of the upper arm.

3. Wires are not pinched between the bottom of the solenoid and the disk drive chassis.

4. Wires do not interfere with solenoid spring.

5.13.13 Drive Motor

To remove the drive motor, proceed as follows:

1. Remove PCBA (refer to paragraph 5.13.1).

2. Place disk drive on its left side.

3. Remove the drive belt by gripping belt near small pulley (motor end); simultaneously pull belt toward spindle pulley and away from the drive chassis. This will rotate belt off spindle pulley. The belt can now be lifted off the motor pulley.

4. Remove two drive motor mounting screws from the bottom of the drive chassis.

5. Drive motor is now free; cut tie wraps holding drive motor wires in harness and pull motor ground spade lug from chassis.

To replace the drive motor, proceed as follows:

1. Perform the preceding steps in the reverse order.

2. Be sure that the wire harness is not pinched between the motor and the chassis.

3. Mount motor so that motor wires exit from rear-center of motor to rear of drive chassis. Tie wrap motor wires into wire harness.

4. After installing belt, refer to table 5-2 for adjustment references.

NOTE

Do not tighten screws in motor mount until belt is adjusted.

5.13.14 Track 00 Sensor

To remove the track 00 sensor, proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).

2. Remove the shield assembly (refer to paragraph 5.13.2).

3. Remove the track 00 photo transistor female connector (top of frame) and track 00 LED female connector (recessed area, bottom of frame).

4. Remove screws (2) at top of chassis holding sensor assembly to the drive chassis.

5. Sensor is now free and can be slid to the side and up out of the drive chassis.

6. Refer to table 5-2 for adjustments necessary.

To replace the track 00 sensor, perform the preceding steps in the reverse order. Do not tighten screws until adjustment procedures referenced in table 5-2 are performed. Note that when replacing the connectors, the connector windows face the chassis.

5.13.15 Door Button Assembly

NOTE

This removal/replacement procedure is associated with the Model 91/92 only. The Model 915/925 is not equipped with a door button assembly.

To remove the door button assembly, proceed as follows. (See figure 5-10.)

1. Remove bezel (refer to paragraph 5.13.5).
2. Remove bezel bracket mounting screw.
3. Remove retention ring from one end of rod.
4. Slide rod from assembly; be sure to catch spring.

To replace the door button assembly, perform the preceding steps in the reverse order.

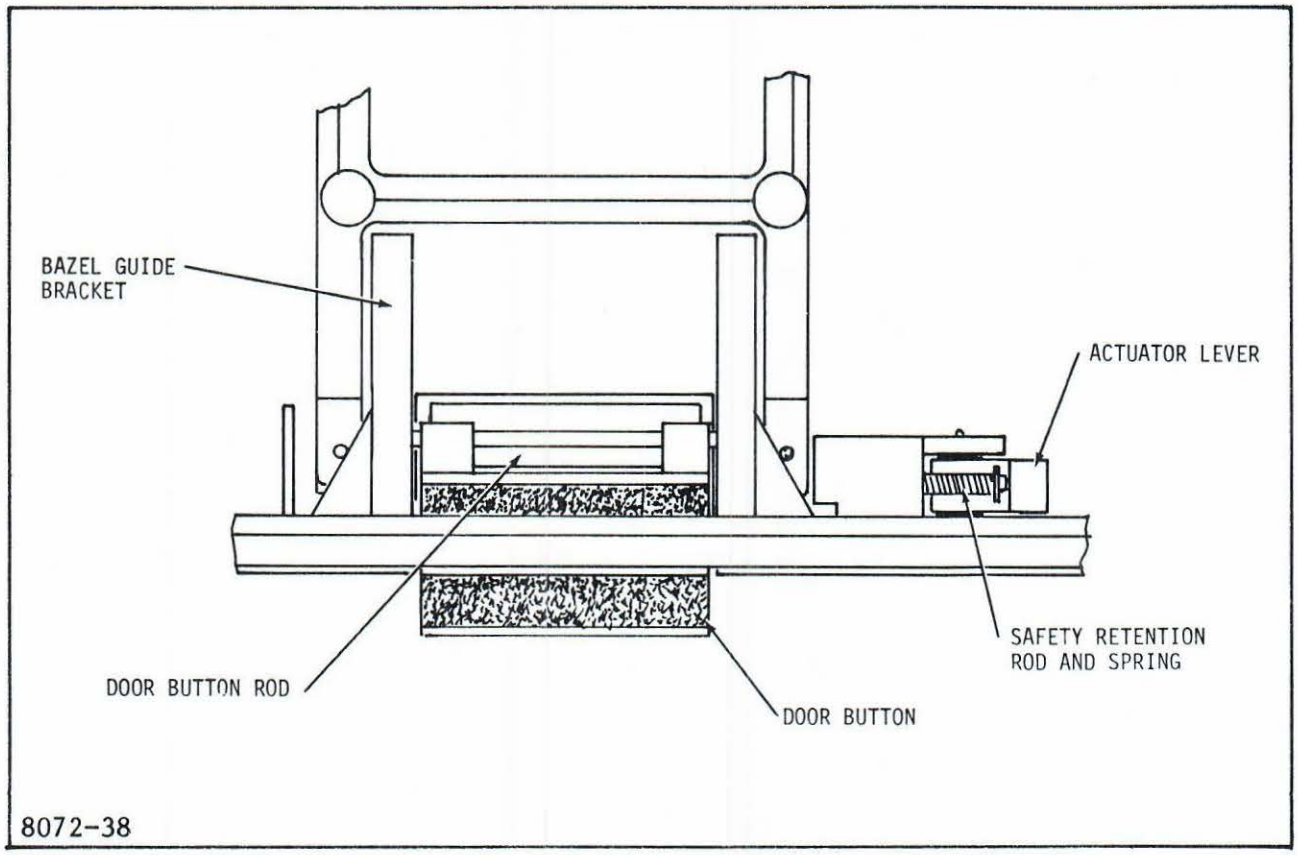


Figure 5-10. Door Button Assembly

5.13.16 Stepper Band

To remove the stepper band (see figure 5-11) proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).
2. Open the door.
3. Remove the left-hand guide (refer to paragraph 5.13.4).
4. Place disk drive on right side.
5. Remove two stepper band mounting screws, washers and band mounting clip from head/carriage assembly. Remove screw mounting band to pulley.
6. Band can now be lifted off stepper motor pulley.

To replace the band, perform the following steps (see figure 5-11):

1. Consider the preceding steps in the reverse order.
2. On the band, slip one head end through the slot in the band.
3. Wrap the band around the pulley.
4. Lay band flat against head/carriage assembly; install screw, washers, and band mounting clip in rear of head/carriage assembly; note large end of band goes to front of drive chassis.

NOTE

The band mounting clip hole is offset. Install the clip so that the hole is closer to the chassis of the disk drive.

5. Hold band firmly against head/carriage assembly; install screw in front of band hole, large end of band.
6. Pull band tight against head/carriage assembly and tighten screw in front of assembly. Move carriage forward and backward. Ensure that there is no band crinkle (metal to metal rubbing).
7. Screws should be tightened with torque screwdriver to 20 inch ounces.

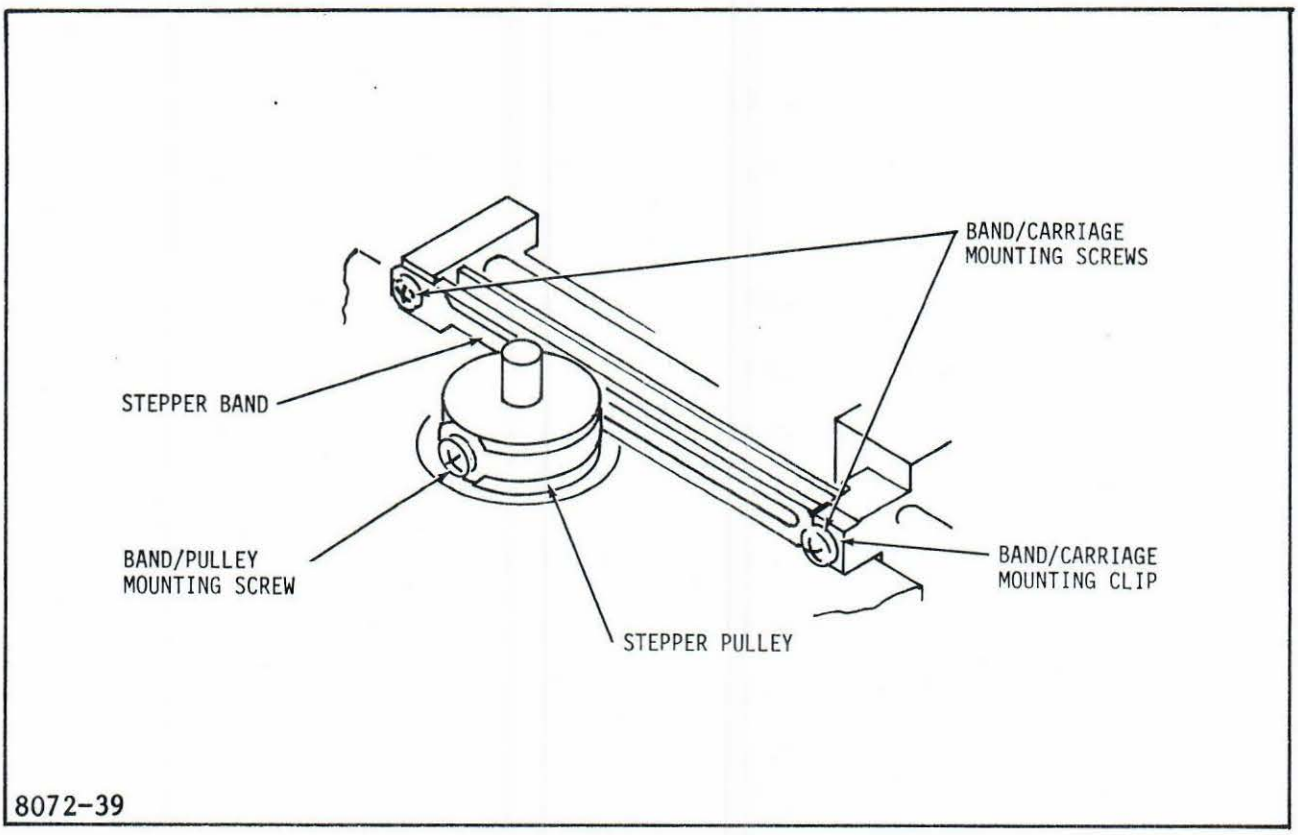


Figure 5-11. Stepper Band

5.13.17 Stepper Motor

To remove the stepper motor, proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).
2. Loosen front band mounting screw.
3. Remove screw mounting band to pulley.
4. Cut tie wraps enclosing stepper motor wires in wire harness.
5. Remove two screws on bottom of drive chassis adjacent to the stepper motor.
6. Remove stepper motor from drive chassis.

To replace the stepper motor, perform the preceding steps in the reverse order. Refer to table 5-2 for required adjustments.

5.13.18 Head/Carriage Assembly

To remove the head/carriage assembly proceed as follows:

1. Remove the PCBA (refer to paragraph 5.13.1).
2. Remove shield assembly (refer to paragraph 5.13.2).
3. Remove left hand guide (refer to paragraph 5.13.4).
4. Remove stepper band (refer to paragraph 5.13.16).
5. Remove head cable clamp from chassis (plastic clamp in left rear of chassis).
6. Loosen the two copper guide rod clamps from front and rear of head assembly by loosening the screws in each of these clamps.
7. Remove left-hand guide rod by prying from front and sliding guide rod out the rear of the chassis.
8. Lift head-carriage assembly off the right-hand guide rod and out of drive chassis.
9. Be careful of banging and bending upper arm leaf spring.

To replace the head/carriage assembly, perform the preceding steps in the reverse order and observe the folowing precautions:

1. Be sure that the guide rods are firmly seated in the drive chassis.
2. Route head cables from head/carriage assembly through chassis properly.
3. Be sure guide rod clamps are securely tightened.
4. Be sure rear clamp has ground lugs (2) secured underneath screw.
5. Be sure carriage rides freely on guide rods after installation.
6. Refer to table 5-2 for required adjustment procedures.

5.13.19 Spindle, Bearings and Pulley

The spindle pulley can be removed by:

1. Removing the spindle drive bolt.
2. Remove the spindle pulley mounting screw.
3. Pull the spindle pulley from the spindle hub shaft.

NOTE

There will be a wave washer and some quantity of shims on the pulley shaft. The same quantity of shims and the wave washer must be replaced in the same order.

NOTE

To replace the spindle and bearings, the unit must be returned to the factory.

5.13.20 Head Load Pad Assembly

To replace the head load pad assembly in Model 91 drives, proceed as follows:

1. Remove PCBA (refer to paragraph 5.13.1).
2. Remove shield (refer to paragraph 5.13.2).
3. Manually position head/carriage assembly all the way to the rear of the drive (Track 00); be sure to push carriage not the upper arm.
4. Open door.
5. Grip upper arm.
6. With bent nose tweezers, squeeze the plastic pieces of the Head Load Pad which protrude through the upper arm and press until it drops out of the upper arm.

To replace the pad assembly proceed as follows:

1. Hold pad assembly with bent nose tweezers centered underneath hole in upper arm.
2. Close door.
3. Press lighly on upper arm to engage pad assembly; remove tweezers.
4. Press on upper arm until pad assembly snaps into place.

CAUTION

Do not move the upper head arm any further than is allowed by the door in its open position.

5. Refer to table 5-2 for required adjustment procedures.

5.13.21 Harness Assembly

It it becomes necessary to replace the harness assembly proceed as follows:

1. Remove PCBA (refer to paragraph 5.13.1), this frees the head connector(s) and PCBA connectors (P4-1, P4-2, and P4-3).

2. Remove connections from:

   a. Bezel activity LED

   b. Right-hand guide write protect sensor (two connections)

   c. Index/load boss sensor

   d. Index LED

   e. Solenoid (two connections)

   f. Track 00 sensor (two connections)

3. All harness connections should now be free.

4. Cut plastic tie wraps which tie harness assembly to drive motor and stepper motor wires.

To replace the harness assembly, perform the preceding steps in the reverse order.

SECTION VI

SPARE PARTS

This section provides a listing of replaceable parts for replacing failed units and for building spares inventories. It contains tabular listings of the field replaceable units, replaceable parts and mounting hardware, keyed to one of four illustrated parts breakdowns.

The following is a listing of recommended field replaceable spares.

Power Supply PCBA

Keyboard Circuit Assembly

Circuit Board #1 (Advanced Video Processor)

Circuit Board #2 (Disk Controller - S/10 Only)

Motherboard

Video Monitor Circuit Assembly

Flyback Transformer

Floppy Disk Drive Assembly

Figures 6-1 thru 6-3 and tables 6-1 thru 6-3 are illustrated parts lists for the ODT and System S/10.

Figure 6-4 in conjunction with tables 6-4 and 6-5 is an illustrated parts list for the S/10 Disk Drive Assembly.

Figures 6-5 and 6-5 are Disk Drive PCB illustrated parts lists.

Figure 6-7 and 6-8 in conjuncton with table 6-6 and 6-7 are Advanced Video Processor Circuit boards and illustrated parts lists.

Figure 6-9 and table 6-8 is the Advanced Floppy Disk Controller Circuit board and illustrated parts list.

Tables 6-9 and 6-10 are the ODT and System S/10 Power Supply Parts List.

Table 6-11 is the Motherboard Parts List.

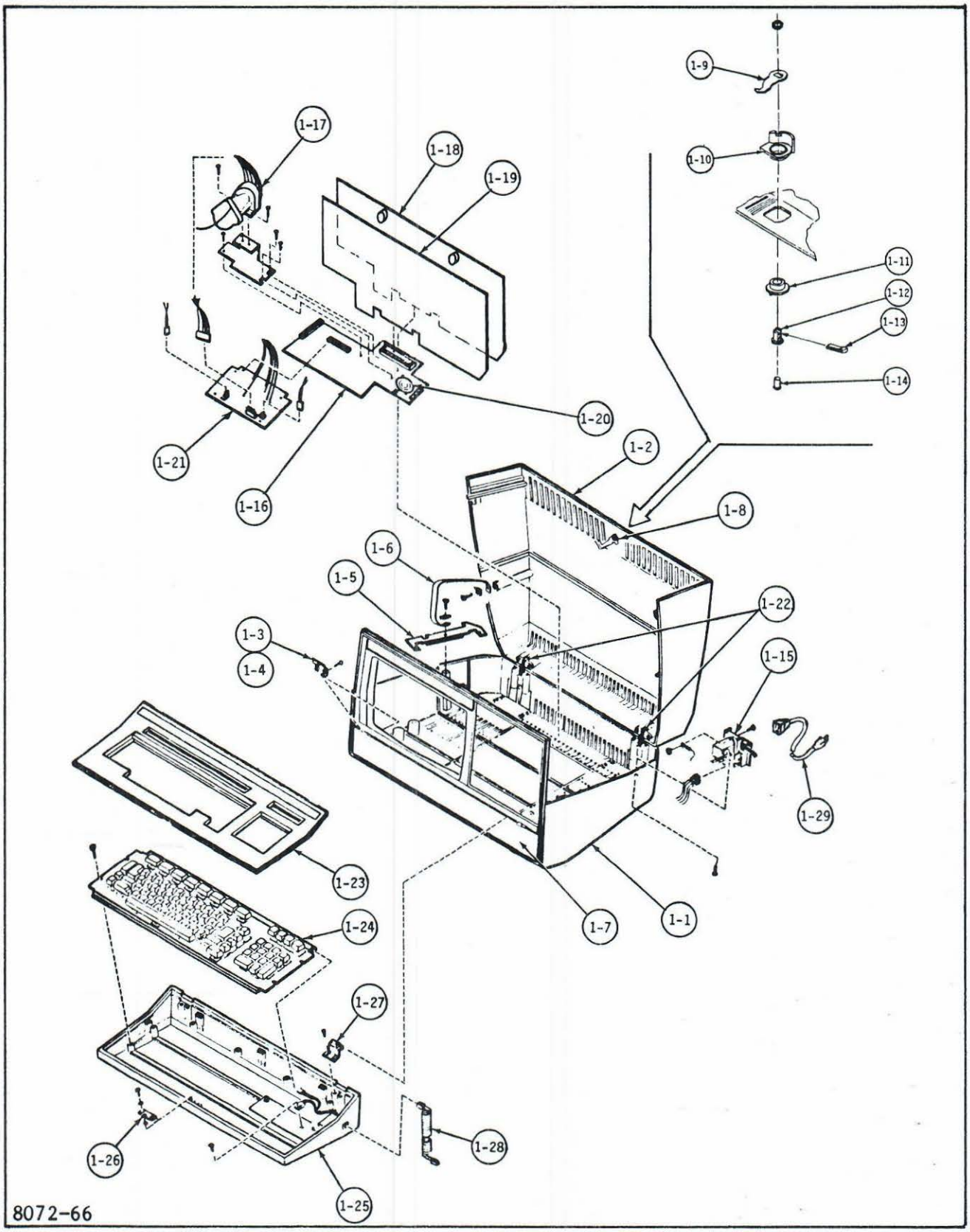


Figure 6-1. ODT - S/10 Keyboard and Cabinet Assembly

Table 6-1. ODT - S/10 Keyboard and Cabinet Assembly

FIG. 6-1 INDEX NO.	DESCRIPTION	ICN DESIGNATION	PART NO.
1-1	BASE ASSEMBLY		000112
1-2	COVER ASSEMBLY		081426
1-3	KEYBOARD MATING HINGE, LEFT		060360
1-4	KEYBOARD MATING HING, RIGHT		060361
1-5	PLATE, POWER SUPPLY HOLDER		060420
1-6	STRAP, STRAIN RELIEF		210044
1-7	FRONT BEZEL, (ODT)		081126
	FRONT BEZE, (S/10)		081127
1-8	LATCH ASSEMBLY		REF.
1-9	LATCH, ARM/COVER LOCKING		060240
1-10	PLATE, CAM		000300
1-11	KNOB, TOP LOCKING		000292
1-12	BARREL, LOCK		060281
1-13	BOLT, LOCK		060291
1-14	PLUG, SCREWDRIVER		060271
1-15	POWER CORD/SWITCH ASSEMBLY	TT528020	081003
1-16	MOTHERBOARD (FIELD REPLACEABLE)	TT520040 (PHASE 1B)	051131 (PHASE 1B)
	MOTHERBOARD (FIELD REPLACEABLE)	TT520041 (PHASE II)	051820 (PHASE II)
1-17	FLYBACK TRANSFORMER, KDS		190040
1-18	ADVANCED FLOPPY CONTROLLER (AFC) PCBA (FIELD REPLACEABLE)	TT520060 (S/10 ONLY)	051301 (S/10 ONLY)

Table 6-1. ODT - S/10 Keyboard and Cabinet Assembly (continued)

FIG. 6-1 INDEX NO.	DESCRIPTION	ICN DESIGNATION	PART NO.
1-19	ADVANCED VIDEO PROCESSOR PCBA, 16K (FIELD REPLACEABLE)	TT520070 (ODT PHASE 1B ONLY)	051281
	ADVANCED VIDEO PROCESSOR PCBA, 64K (FIELD REPLACEABLE)	TT520050 (S/10 PHASE 1B ONLY)	051310
	ADVANCED VIDEO PROCESSOR PCBA, 16K (FIELD REPLACEABLE)	TT520071 (ODT PHASE II ONLY)	051901
	ADVANCED VIDEO PROCESSOR PCBA, 64K (FIELD REPLACEABLE)	TT520051 (S/10 PHASE II ONLY)	051950
1-20	SPEAKER		130001
1-21	VIDEO MONITOR BOARD (FIELD REPLACEABLE)	TT520130	190038
1-22	HINGE, CASE MAIN		180001
1-23	KEYBOARD COVER		000162
1-24	KEYBOARD CIRCUIT ASSEMBLY (FIELD REPLACEABLE)	TT523010 (PHASE 1B)	
1-25	KEYBOARD BASE ASSEMBLY	TT523100 (PHASE II)	081035
1-26	KEYBOARD LATCH PLATE		060130
1-27	KEYBOARD HINGE ASSY. (RIGHT SIDE)		081140
	KEYBOARD HINGE ASSY. (LEFT SIDE)		081130
1-28	KEYBOARD CABLE	TT528050	300001
1-29	POWER CORD	TT528090	300002

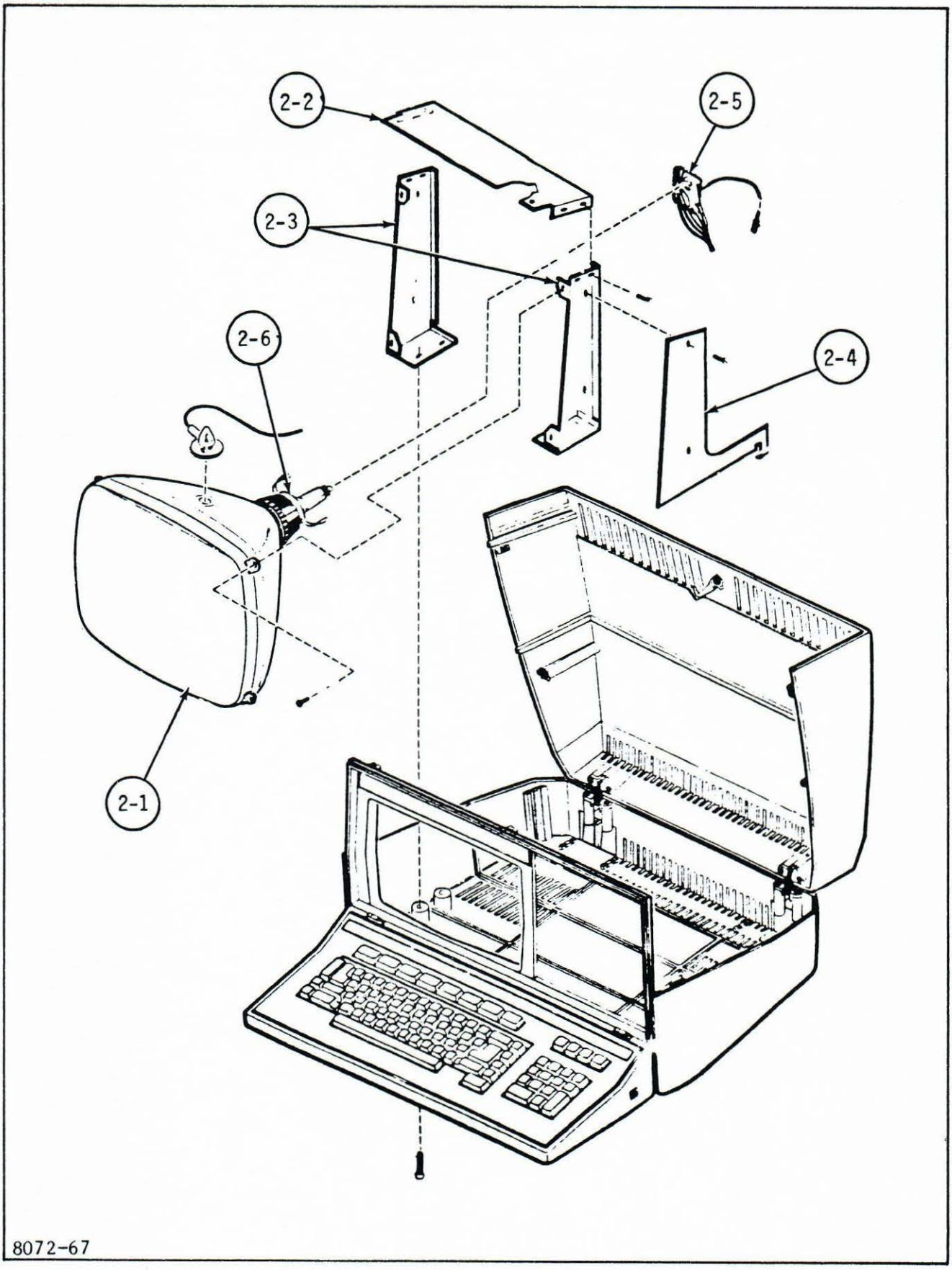


Figure 6-2. ODT - S/10 CRT Assembly

Table 6-2. ODT - S/10 CRT Assembly

FIG. 6-2 INDEX NO.	DESCRIPTION	ICN DESIGNATION	PART NO.
2-1	CRT, 12 VOLT, KDS ASSEMBLY	TT527010 (PHASE 1B AND PHASE II)	081305
2-2	CHASSIS, TOP		
2-3	CHASSIS, SIDE (LEFT)		060401
	CHASSIS, SIDE (RIGHT)		060400
2-4	CHASSIS, BRACKET SUPPORT		060491
2-5	CRT CONNECTOR BOARD		
2-6	YOKE, KDS CRT		190039

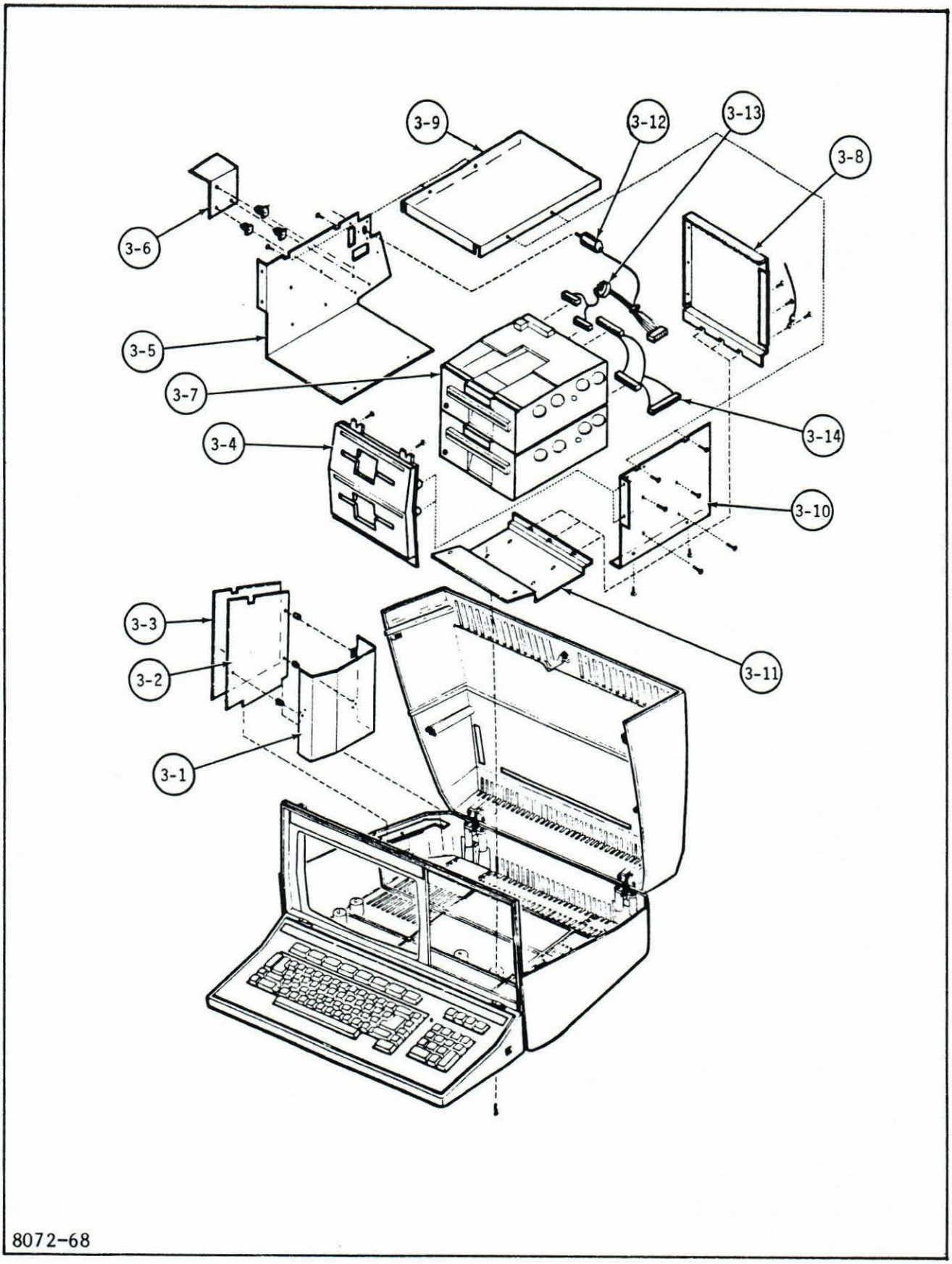


Figure 6-3. S/10 Disk Drive Assembly

Table 6-3. S/10 Disk Drive Assembly

FIG. 6-3 INDEX NO.	DESCRIPTION	ICN DESIGNATION	PART NO.
3-1	SHIELD, POWER SUPPLY		060390
3-2	POWER SUPPLY PCBA	TT527010 (S/10 PHASE 1B ONLY)	200008
	POWER SUPPLY PCBA	TT527020 (ODT PHASE 1B ONLY)	200000
	POWER SUPPLY PCBA (100 WATT)	TT527011	081642 (S/10 ONLY PHASE II)
	POWER SUPPLY PCBA (60 WATT)	TT527021	081643 (ODT ONLY PHASE II)
3-3	INSULATOR, POWER SUPPLY ASSEMBLY		000890
3-4	FRONT PANEL, DISK DRIVE		000460
3-5	BRACKET, DISK DRIVE, LEFT		060430
3-6	BRACKET, FLYBACK TRANSFORMER SHIELD		060540
3-7	DISK DRIVE ASSEMBLY (33 min) DISK DRIVE ASSEMBLY (0 min)	TT524010 TT524070	081451
3-8	COVER, DISK DRIVE REAR SHIELD		060550
3-9	COVER, DISK DRIVE TOP		081451
3-10	BRACKET, DISK DRIVE, RIGHT		060440
3-11	BRACKET, DISK DRIVE, BOTTOM		081450
3-12	MOTOR, COOLING FAN		130009
	BLADE, FAN		130010
3-13	CABLE ASSEMBLY, DISK DRIVE POWER		081440
3-14	CABLE ASSEMBLY, DISK DRIVE INTERFACE		081430
REF	CONNECTOR, 34 PIN CARD EDGE, J2, J3		210036
REF	CONNECTOR, 34 PIN SOCKET, J1		210037

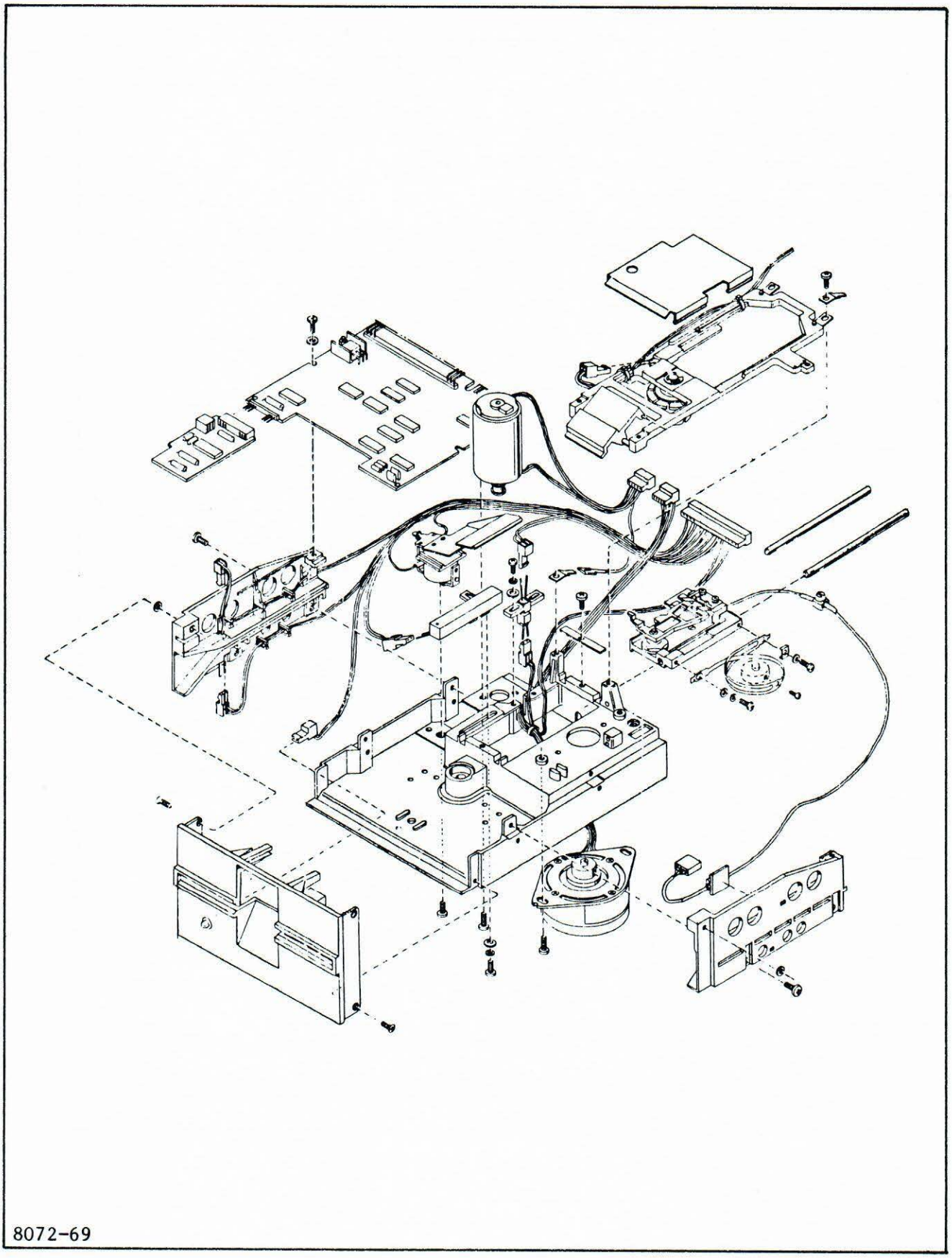


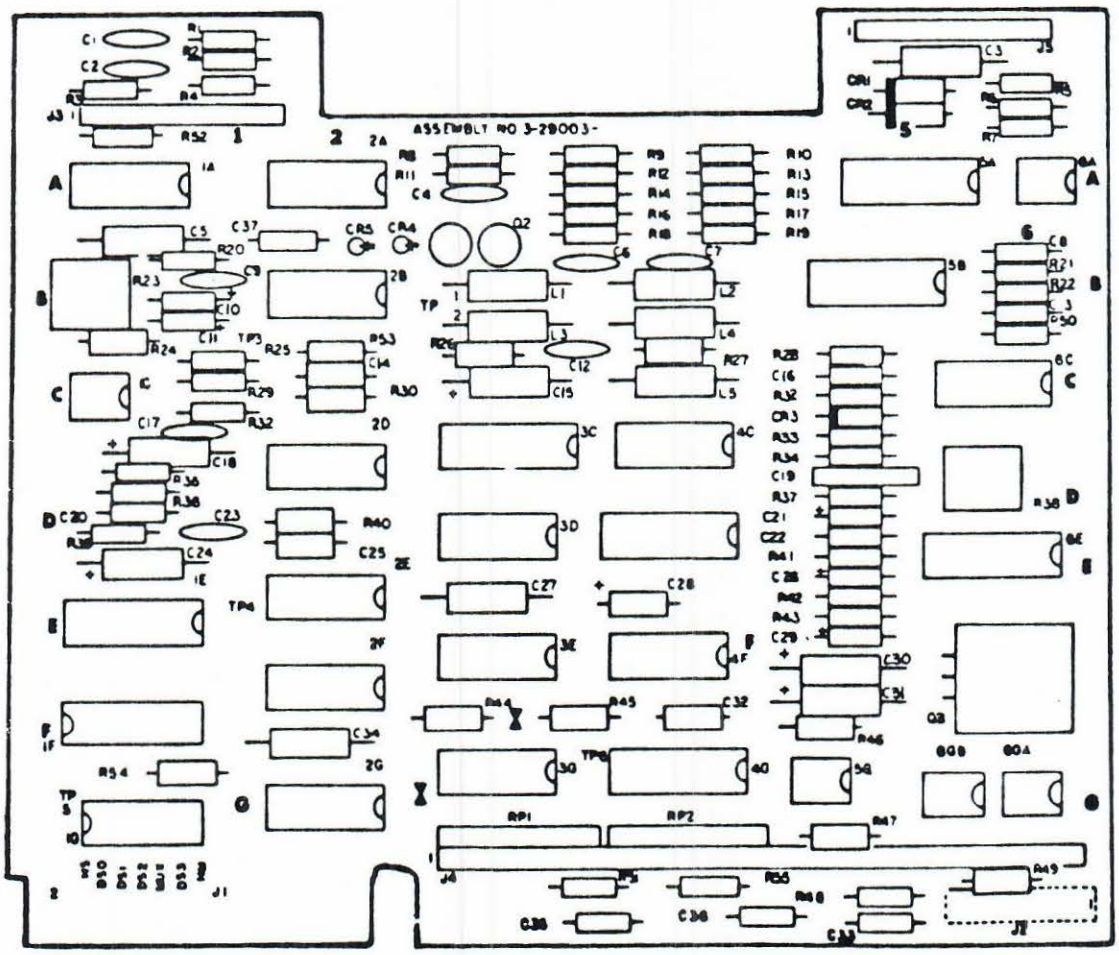
Figure 6-4. Disk Drive, Exploded View

Table 6-4. Disk Drive Model 915/925 Recommended Spare Parts List

MPI P/N	DESCRIPTION
1. REPLACEABLE PARTS AND SUB ASSEMBLIES	
3-29003-XXX	PCB Assembly
1-79600-006	Shunt
3-35003-001	Spindle Drive Motor Assembly
2-35039-001	Stepper Motor Assembly
4-27053-001	Stepper Band
2-32002-002	Head Load Solenoid Assembly
2-35000-002	Track 00 Assembly
2-35032-001	Shield Assembly
3-35006-002	Rt Hand Guide/Write Protect Assy
4-21013-006	Lt Hand Guide
1-35028-001	Cone/Clutch Assembly
3-22016-001	Spindle Pulley
4-35009-001	Carriage/Head Assembly (Single, 91/91S)
4-35034-001	Carriage/Head Assembly (Double, 92/92S)
3-32003-004	Harness Assembly
1-50500-001	Drive Belt - Neoprene (Black)
2-35001-004	Index/Load Boss Assembly
1-35045-001	Door/Carrier Assembly (SLA)
1-35029-001	Door/Carrier Assembly (MPI)
1-35023-001	Load Pad Assembly (91/91S)
1-35026-001	Indicator L.E.D. Assembly
1-77004-151	Terminator - 150 Pullup
1-77005-001	Terminator - 220 /330
3-35040-001	Bezel Assembly (SLA)
4-21014-001	Bezel (MPI)
1-35048-001	Ejector Mechanism Assembly (MPI)
NOTE: READILY AVAILABLE COMPONENTS AND HARDWARE NOT INCLUDED	

Table 6-4. Disk Drive Model 915/925 Recommended Spare Parts List (continued)

MPI P/N	DESCRIPTION
II. COMPONENTS	
1-76000-010	IC, 74LS10
1-76000-014	IC, 74LS14
1-76000-033	IC, 74LS33
1-76000-074	IC, 74LS74
1-76000-086	IC, 74LS86
1-76000-123	IC, 74LS123
1-76000-139	IC, 74LS139
1-76000-169	IC, 74LS169
1-76001-038	IC, 7438
1-76004-463	IC, 75463
1-76006-311	IC, LM311
1-76006-339	IC, LM339
1-76005-054	IC, CA3054
1-76007-592	IC, NE592
1-76004-478	IC, 75478
1-76008-001	IC, 7391
1-78501-001	Transistor, 2N3904
1-78503-001	Transistor, TIP 110
1-75000-150	Diode, IN4150
1-77000-223	Resistor DIP, 22K
1-77002-151	Resistor SIP, 150
1-77002-472	Resistor SIP, 4.7K
1-79000-103	Pot, 10K
1-79001-503	Pot, 50K
1-78001-151	Inductor, 150uH
1-78001-561	Inductor, 560uH
1-78001-331	Inductor, 330uH
III. SPECIAL TOOLS	



TPS/10-30

Figure 6-5. Disk Drive PCBA Component Layout

Table 6-5. Disk Drive PCBA Component Layout

I.C. DESIGNATOR	TYPE	P/N
1A, 2A	CA3054	1-76005-054
1C	LM311	1-76006-311
1E,5B,6E	74LS123	1-76000-123
2B	NE592	1-76007-592
2D	74LS86	1-76000-086
2E	74LS74	1-76000-074
2F,3D,3G	74LS14	1-76000-014
2G,3E	7438	1-76001-038
3C	74LS169	1-76000-169
4C	74LS10	1-76000-010
4F	LM339	1-76006-339
5A	74LS139	1-76000-139
5G	75478	1-76004-478
6A	75463	1-76004-463
6C	74LS33	1-76000-033
6Ga,6Gb	75478	1-76004-478

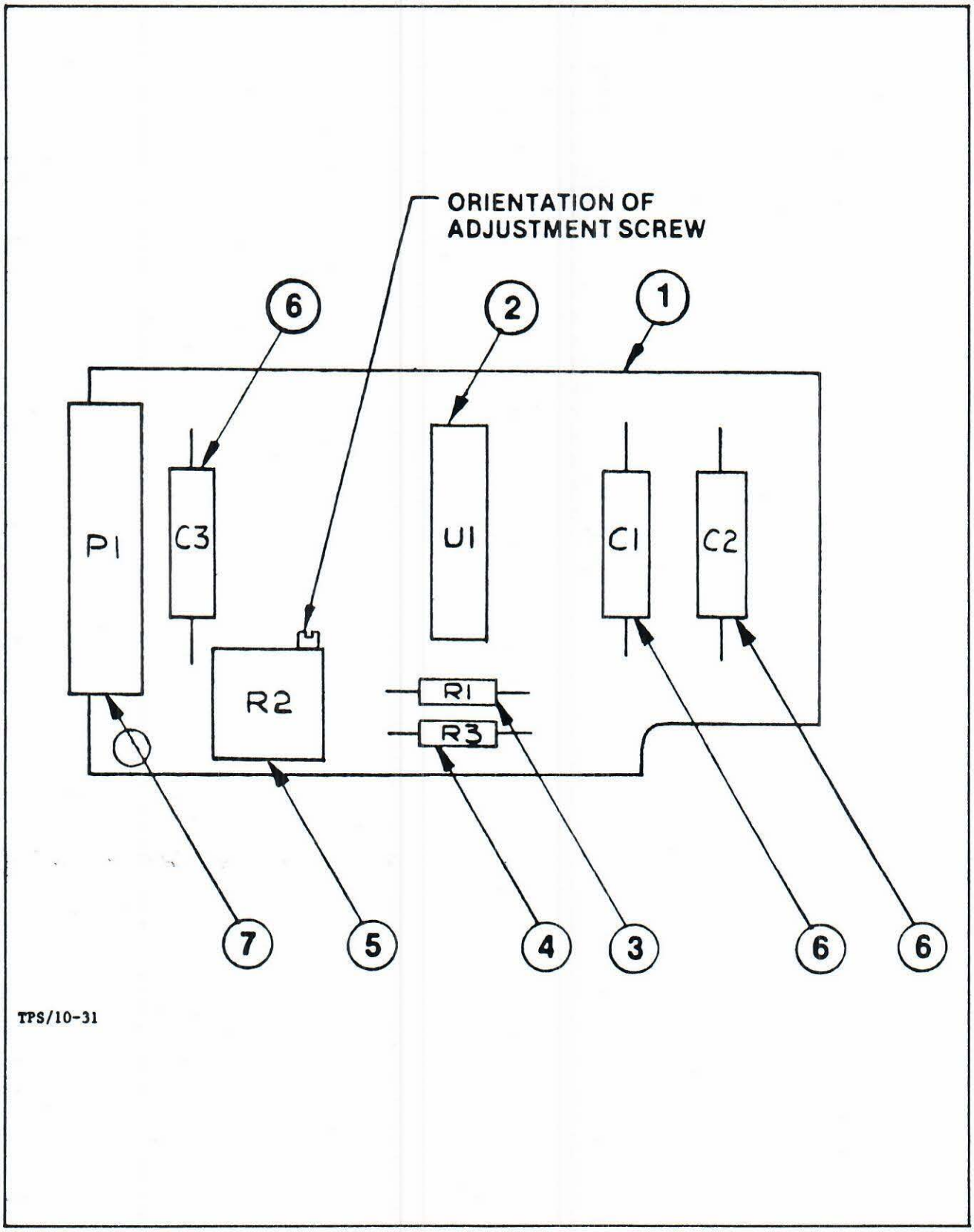


Figure 6-6. Disk Drive Ready PCBA Component Layout

Table 6-6. Disk Drive Ready PCBA Component Layout

REFERENCE NUMBER	PART NUMBER	DESCRIPTION
1	2-28013-003	PCB, Ready Logic
2	1-76000-123	I.C., 74LS123
3	1-77003-103	RESISTOR, 10K, 1/4 W, 5%
4	1-77003-563	RESISTOR, 56K, 1/4 W, 5%
5	1-79001-503	POTENTIOMETER, 50K
6	1-74014-156	CAPACITOR, 15 uf, 16V Electrolytic
7	1-60006-001	CONNECTOR, PCB Mount

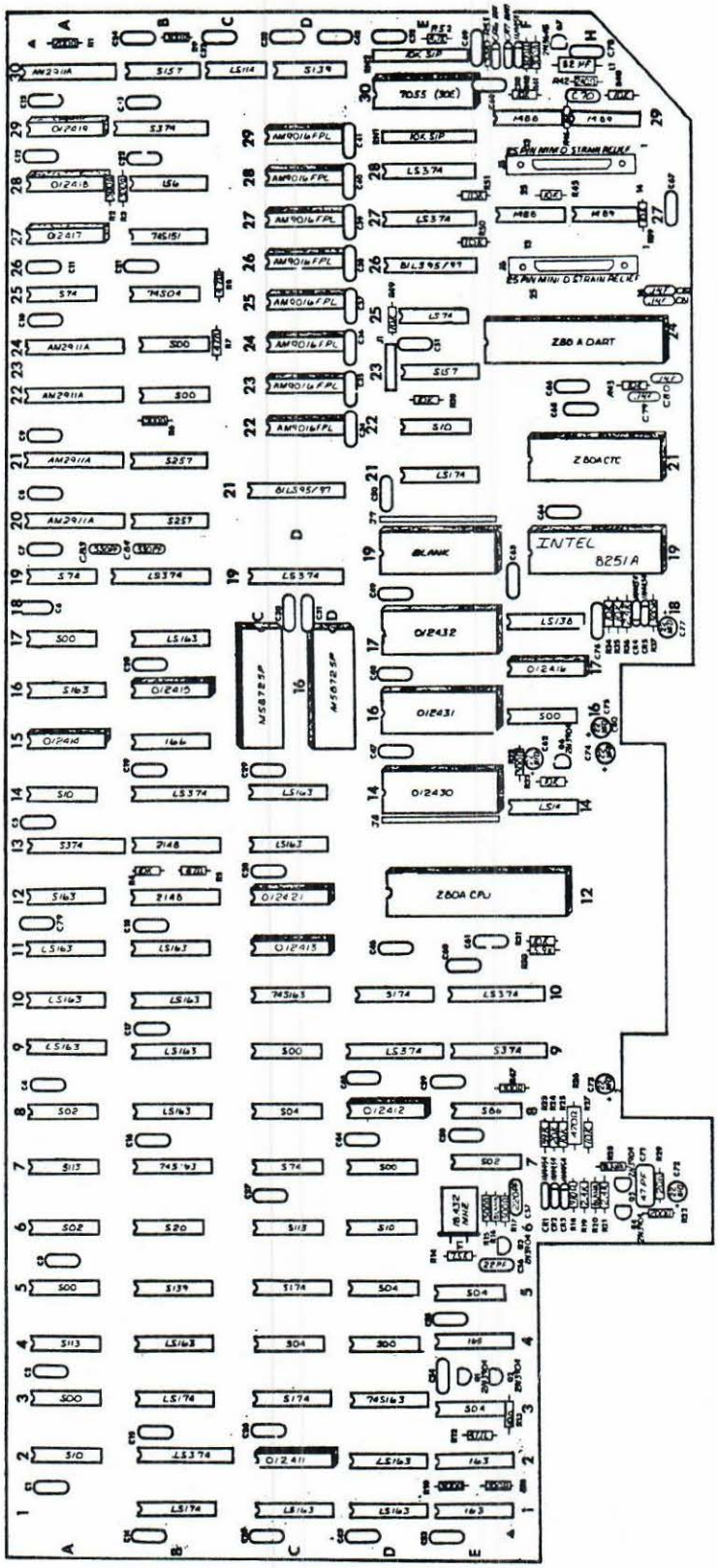


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Figure 6-7. Advanced Video Processor Circuit Board Assembly Diagram AVP - (ODT ONLY)

Table 6-7. Advanced Video Processor, (16K) Parts List (Used on ODT System)
TT520070 P/N 051281 (Phase 1B)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
1	YY003792	1	130003	CRYSTAL: 18.432 MHZ	Y1
2	YY010942	1	130007	COIL: 82MH	L1
3	YY010754	73	151040	CAP: .1 MF 50V	C1 THRU C55, C58 THRU C61, C63 THRU C70, C76, C78 THRU C82
4	YY010798	1	152200	CAP: 22 PF 50V	C56
5	YY010799	1	152210	CAP: 220 PF 50V	C57
6	YY010800	6	152262	CAP: 22MF GUMDROP ELEC 15V	C62, C72, C73, C74, C75, C77
7	YY010756	2	153310	CAP: 330 PF 50V	C83, C84
8	YY010800	1	154700	CAP: 47 PF 50V	C71
9	YY010779	2	230001	IC: 81LS95/97 OCTL BUFF	21D, 26E
10	YY010780	5	230005	IC: 2911 BIPOL 4BIT U-SEQ	20A, 21A, 22A, 24A, 30A
11	OR999397	2	230008	IC: 1489BIPOL RS232 TTL TR	27H, 29H
12	OR999398	2	230009	IC: 1488BIPOL TT1-RS232	27F, 29F
13	YY010963	2	230016	IC: 2148H 3BIPOL 255X4	12B, 13B
14	YY005329	1	231156	IC: 74156 DUAL 1 OF 4 DC	28B
15	YY000163	3	231163	IC: 74163 4BIT CTR BIN SYN	1E, 2E, 4E
16	YY002687	1	231166	IC: 74166 8BIT SHF RGTR	15B
17	YY003577	1	232014	IC: 74LS14 HEX SCHM TRG INV	14F

Table 6-7. Advanced Video Processor, (16K) Parts List (Used on ODT System) TT520070 P/N 051281 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
18	YY000442	1	232074	IC: 74LS74 DUAL D FLIP-FLOP	25E
19	YY004412	1	232114	IC: 74LS114 DUAL JK NEG F/F	30C
20	YY003584	1	232138	IC: 74LS138 3 TO 8 DCDR MUX	18F
21	YY005908	14	232163	IC: 74LS163 4BIT BIN CTR	4B, 8B THRU 11B, 1C, 1D, 2D, 13C, 14C, 17B, 9A THRU 11A
22	YY000446	3	232174	IC: 74LS174 HEX D FLIP-FLOP	1B, 3B, 21E
23	YY003597	8	232374	IC: 74LS374 OCT D FLIP-FLOP	2B, 14B, 19B, 9D, 19D, 10E, 27E, 28E
24	YY000041	9	233000	IC: 74S00 QUAD2 INP + NG	3A, 5A, 17A, 22B, 24B, 9C, 4D, 7D, 16F
25	YY003044	3	233002	IC: 74S02 QUAD 2 INP + NG	6A, 8A, 7E
26	YY000027	6	233004	IC: 74S04 HEX INVERTERS	25B, 4C, 8C, 5D, 3E, 5E
27	YY000022	4	233010	IC: 74S10 TRI 3 INP + NG	2A, 14A, 6D, 22E
28	BB000189	1	233020	IC: 74S20 DUAL 4 INP + NG	6B
29	YY000746	3	233074	IC: 74S74 DUAL D + TRIG F/F	19A, 25A, 7C
30	YY003561	1	233086	IC: 74S86 QUAD 2 INP EXCLUE	8E
31	YY004152	3	233113	IC: 74S113 DUAL JK TRIG F/F	4A, 7A, 6C
32	YY003076	2	233139	IC: 74S139 DUAL 1:4 DCDR	5B, 30D
33	YY005319	1	233151	IC: 74S151 1 TO 8 MUX	27B

Table 6-7. Advanced Video Processor, (16K) Parts List (Used on ODT System) TT520070 P/N 051281 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
34	YY003038	2	233157	IC: 74S157 QUAD 2 TO 1 MUX	23E, 30B
35	YY002873	5	233163	IC: 74S163 4BIT CRT BIN SIN	16A, 12A. 7B, 10C, 3D
36	YY004808	3	233174	IC: 74S174 HEX D FLIP/FLOP	3C, 5C, 10D
37	YY005909	2	233257	IC: 74S257 QUAD 2 INP MUX	20B, 21B
38	YY003575	3	233374	IC: 74S374 OCT D FLIP/FLOP	13A, 29B, 9E
39	YY007837	1	271000	R: 10 OHM 5% 1/4 W	R13
40	YY000127	16	271030	R: 10K OHM 5% 1/4 W CC	R4, R25, R27, R31, R33 THRU R35, R38, R39,R40, R43, R45, R46, R49, R50, R51
41	YY010749	2	271032	R: NETWORK 10K SIP	RN1, RN2
42	YY006917	1	272000	R: 20 OHM 5% 1/4W CC	R29
43	YY000064	2	272010	R; 200 OHM 5% 1/4W CC	R22, R1
44	0T001288	1	272030	R: 20K OHM 5% 1/4 W CC	R24
45	YY000830	1	272410	R: 240 OHM 5% 1/4 W CC	R42
46	YY010750	3	272420	R: 2.4K OHM 5% 1/4 W CC	R19, R21, R36
47	YY000119	12	273010	R: 300 OHM 5% 1/4 W CC	R2, R3, R6, R10, R11, R15, R17, R32 R48, R41, R47, R9
48	YY006891	1	273040	R: 300K OHM 5% 1/4 W CC	R37
49	YY000876	1	273920	R: 3.9K OHM 5% 1/4 W CC	R30
50	YY000116	1	273930	R: 39K OHM 5% 1/4 W CC	R23

Table 6-7. Advanced Video Processor, (16K) Parts List (Used on ODT System) TT520070 P/N 051281 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
51	OT000368	4	274700	R: 47 OHM 5% 1/4 W CC	R5, R7, R8, R12
52	OT000314	1	274711	R: 470 OHM 5% 1/2 W CC	R26
53	YY000127	1	274720	R: 4.7K OHM 5% 1/4 W CC	R52
54	YY007802	2	277520	R: 7.5K OHM 5% 1/4 W CC	R14, R53
55	YY005524	1	279110	R: 910 OHM 5% 1/4 W CC	R18
56	YY000350	1	283645	T: PNP 2N3645	Q7
57	YY000767	6	283904	T: 2N3904	Q1 THRU Q6
58	YY000187	6	284454	DIODE: 1N4454	CR1 THRU CR5, CR8
59	YY010943	1	284745	DIODE: ZENER 1N4745 16V	CR6
60	YY002819	1	284746	DIODE: ZENER 1N4746 18V	CR7
61	YY011295	1	012411	IC: AVP VERT TIME CNTRLR TBP24S10N	2C
62	YY011296	1	012412	IC: AVP VID ATT CNTRLR TBP24S10N	8D
63	YY011297	1	012413	IC: AVP FONT WIDTH CNTRLR TBP18S030N	11C
64	YY011298	1	012414	IC: AVP LINE BUFFER CNTRL TBP18S030N	15A
65	YY011299	1	012415	IC: AVP EOL CNTRLR TBP24S10N	16B
66	YY011300	1	012416	IC: AVP EROM CNTRLR 74S288	17F
67	YY011301	1	012417	IC: AVP DMA-1 TBP18S030N	27A
68	YY011302	1	012418	IC: AVP DMA-2 TBP18S030N	28A

Table 6-7. Advanced Video Processor, (16K) Parts List (Used on ODT System) TT520070 P/N 051281 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
69	YY011303	1	012419	P: AVP DMA-3 TBP18S030N	29A
70	YY011304	1	012421	P: AVP CD TBP24S10N	12C
71	YY010756	1	153310	CAP: 330 PF 50V	C83
72	YY011307	1	230002	IC: 8251A MOS UART	19F
73	YY005931	1	230011	IC: Z80A MICRO PROC CPU	12E
74	YY010906	1	230012	IC: 2055 64X8 MNOS ROM	30E
75	YY011319	1	230026	IC: Z80A DART	24F
76	YY005930	1	230029	IC: Z80A CTC CNTRL CRCT	21F
77	YY011309	2	230034	IC: M58725P 2K X 8 RAM	16C, 16D
78	YY011320	8	230036	IC: 16K X 1 RAM 150 NS	22D THRU 29D
79	YY011321	1	012430	IC: AVP BOOT 2732A EPROM	14E
80	YY011322	1	012431	IC: AVP BOOT 2732A EPROM	16E
81	YY011323	1	012432	IC: AVP BOOT 2732A EPROM	17E

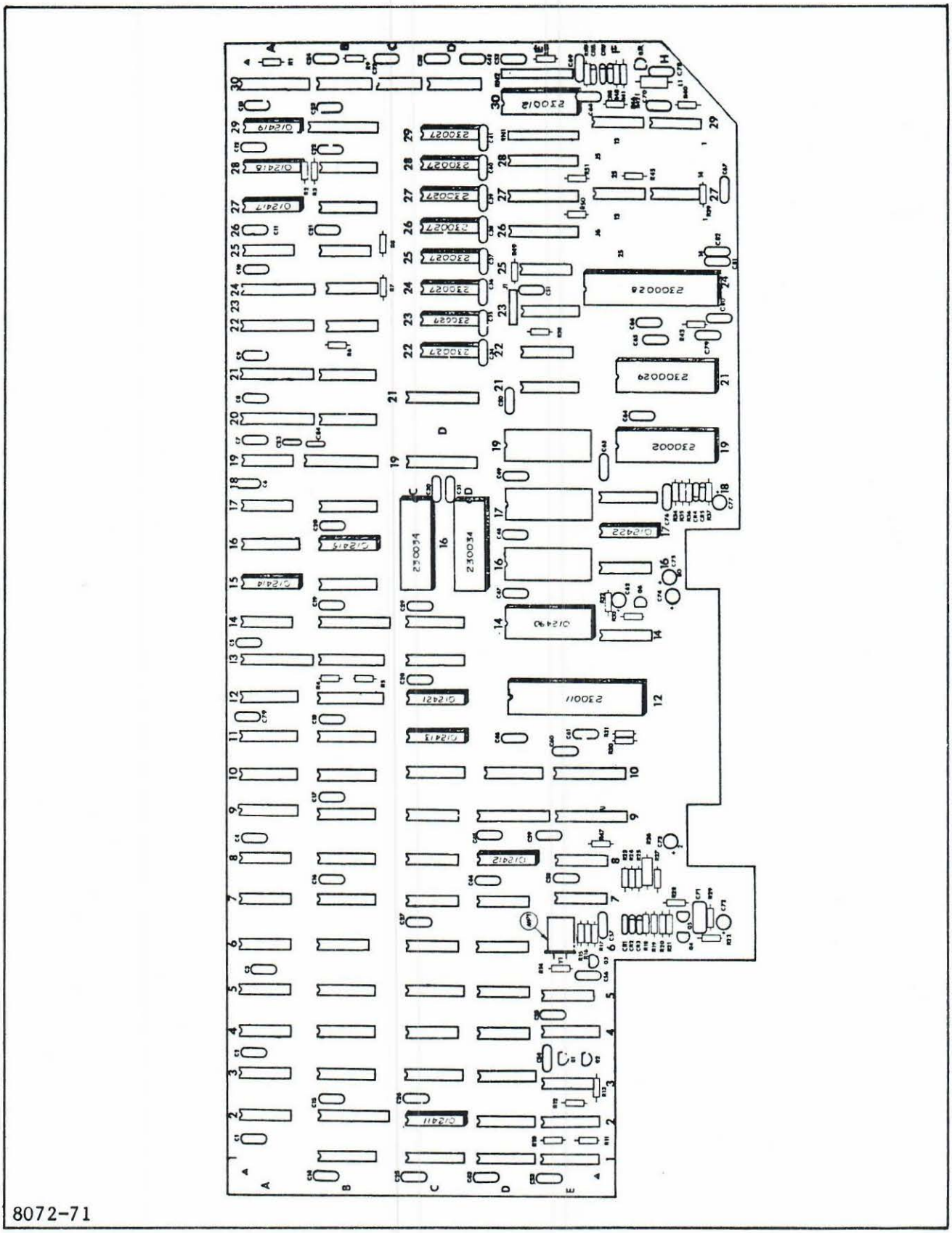

Figure 6-8. Advanced Video Processor Circuit Board Assembly Diagram, AVP - (S/10 Only)

Table 6-8. Advanced Video Processor, (64K) Parts List (Used on S/10 System)
TT520050 P/N 051310 (Phase 1B)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
1	YY003792	1	130003	CRYSTAL: 18.432 MHZ	Y1
2	YY010942	1	130007	COIL: 82MH	L1
3	YY010754	73	151040	CAP: .1 MF 50V	C1 THRU C55, C58 THRU C61, C63 THRU C70, C76, C78 THRU C82
4	YY010789	1	152200	CAP: 22 PF 50V	C56
5	YY010799	1	152210	CAP: 220 PF 50V	C57
6	YY010800	6	152262	CAP: 22MF GUMDROP ELEC 15V	C62, C72, C73, C74, C75, C77
7	YY010756	2	153310	CAP: 330 PF 50V	C83, C84
8	YY010800	1	154700	CAP: 47 PF 50V	C71
9	YY010779	2	230001	IC: 81LS95/97 OCTL BUFF	21D, 26E
10	YY010780	5	230005	IC: 2911 BIPOL 4BIT U-SEQ	20A, 21A, 22A, 24A, 30A
11	OR999397	2	230008	IC: 1489BIPOL RS232 TTL TR	27H, 29H
12	OR999398	2	230009	IC: 1488BIPOL TT1-RS232	27F, 29F
13	YY010963	2	230016	IC: 2148H 3BIPOL 255X4	12B, 13B
14	YY005329	1	231156	IC: 74156 DUAL 1 OF 4 DC	28B
15	YY000163	3	231163	IC: 74163 4BIT CTR BIN SYN	1E, 2E, 4E
16	YY002687	1	231166	IC: 74166 8BIT SHF RGTR	15B
17	YY003577	1	232014	IC: 74LS14 HEX SCHM TRG INV	14F

Table 6-8. Advanced Video Processor, (64K) Parts List (Used on S/10 System) TT520050 P/N 051310 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
18	YY000442	1	232074	IC: 74LS74 DUAL D FLIP-FLOP	25E
19	YY004412	1	232114	IC: 74LS114 DUAL JK NEG F/F	30C
20	YY003584	1	232138	IC: 74LS138 3 TO 8 DCDR MUX	18F
21	YY005908	14	232163	IC: 74LS163 4BIT BIN CTR	4B, 8B THRU 11B, 1C, 1D, 2D, 13C, 14C, 17B, 9A THRU 11A
22	YY000446	3	232174	IC: 74LS174 HEX D FLIP-FLOP	1B, 3B, 21E
23	YY003597	8	232374	IC: 74LS374 OCT D FLIP-FLOP	2B, 14B, 19B, 9D, 19D, 10E, 27E, 28E
24	YY000041	9	233000	IC: 74S00 QUAD2 INP + NG	3A, 5A, 17A, 22B, 24B, 9C, 4D, 7D, 16F
25	YY003044	3	233002	IC: 74S02 QUAD 2 INP + NG	6A, 8A, 7E
26	YY000027	6	233004	IC: 74S04 HEX INVERTERS	25B, 4C, 8C, 5D, 3E, 5E
27	YY000022	4	233010	IC: 74S10 TRI 3 INP + NG	2A, 14A, 6D, 22E
28	BB000189	1	233020	IC: 74S20 DUAL 4 INP + NG	6B
29	YY000746	3	233074	IC: 74S74 DUAL D + TRIG F/F	19A, 25A, 7C
30	YY003561	1	233086	IC: 74S86 QUAD 2 INP EXCLUE	8E
31	YY004152	3	233113	IC: 74S113 DUAL JK TRIG F/F	4A, 7A, 6C
32	YY003076	2	233139	IC: 74S139 DUAL 1:4 DCDR	5B, 30D
33	YY005319	1	233151	IC: 74S151 1 TO 8 MUX	27B

Table 6-8. Advanced Video Processor, (64K) Parts List (Used on S/10 System) TT520050 P/N 051310 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
34	YY003038	2	233157	IC: 74S157 QUAD 2 TO 1 MUX	23E, 30B
35	YY002873	5	233163	IC: 74S163 4BIT CRT BIN SIN	16A, 12A, 7B, 10C, 3D
36	YY004808	3	233174	IC: 74S174 HEX D FLIP/FLOP	3C, 5C, 10D
37	YY005909	2	233257	IC: 74S257 QUAD 2 INP MUX	20B, 21B
38	YY003575	3	233374	IC: 74S374 OCT D FLIP/FLOP	13A, 29B, 9E
39	YY007837	1	271000	R: 10 OHM 5% 1/4 W	R13
40	YY000127	16	271030	R: 10K OHM 5% 1/4 W CC	R4, R25, R27, R31, R33 THRU R35, R38, R39, R40, R43, R45, R46, R49, R50, R51
41	YY010749	2	271032	R: NETWORK 10K SIP	RN1, RN2
42	YY006917	1	272000	R: 20 OHM 5% 1/4W CC	R29
43	YY000064	2	272010	R; 200 OHM 5% 1/4W CC	R22, R1
44	OT001288	1	272030	R: 20K OHM 5% 1/4 W CC	R24
45	YY000830	1	272410	R: 240 OHM 5% 1/4 W CC	R42
46	YY010750	3	272420	R: 2.4K OHM 5% 1/4 W CC	R19, R21, R36
47	YY000119	12	273010	R: 300 OHM 5% 1/4 W CC	R2, R3, R6, R10, R11, R15, R17, R32 R48, R41, R47, R9
48	YY006891	1	273040	R: 300K OHM 5% 1/4 W CC	R37
49	YY000876	1	273920	R: 3.9K OHM 5% 1/4 W CC	R30
50	YY000116	1	273930	R: 39K OHM 5% 1/4 W CC	R23

Table 6-8. Advanced Video Processor, (64K) Parts List (Used on S/10 System) TT520050 P/N 051310 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
51	OT000368	4	274700	R: 47 OHM 5% 1/4 W CC	R5, R7, R8, R12
52	OT000314	1	274711	R: 470 OHM 5% 1/2 W CC	R26
53	YY000127	1	274720	R: 4.7K OHM 5% 1/4 W CC	R52
54	YY007802	2	277520	R: 7.5K OHM 5% 1/4 W CC	R14, R53
55	YY005524	1	279110	R: 910 OHM 5% 1/4 W CC	R18
56	YY000350	1	283645	T: PNP 2N3645	Q7
57	YY000767	6	283904	T: 2N3904	Q1 THRU Q6
58	YY000187	6	284454	DIODE: 1N4454	CR1 THRU CR5, CR8
59	YY010943	1	284745	DIODE: ZENER 1N4745 16V	CR6
60	YY002819	1	284746	DIODE: ZENER 1N4746 18V	CR7
61	YY011295	1	012411	IC: AVP VERT TIME CNTRLR 74S287	2C
62	YY011296	1	012412	IC: AVP VID ATT CNTRLR 74S287	8D
63	YY011297	1	012413	IC: AVP FONT WIDTH CNTRLR 74S288	11C
64	YY011298	1	012414	IC: AVP LINE BUFFER CNTRL 74S288	15A
65	YY011299	1	012415	IC: AVP EOL CNTRLR 74S287	16B
66	YY011301	1	012417	IC: AVP DMA-1 74S287	27A
67	YY011302	1	012418	IC: AVP DMA-2 74S288	28A
68	YY011303	1	012419	IC: AVP DMA-3 74S288	29A
69	YY011304	1	012421	IC: AVP CD DM 74S287	12C

Table 6-8. Advanced Video Processor, (64K) Parts List (Used on S/10 System) TT520050 P/N 051310 (Phase 1B) (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
70	YY011305	1	012422	IC: AVP CPM ROM CNTRL 74S288	17F
71	YY011306	1	012490	IC: AVP BOOT 2764A	14E
72	YY011307	1	230002	IC: 8251A MOS UART	19F
73	YY005931	1	230011	IC: Z80A MICRO PROC CPU	12E
74	YY010906	1	230012	IC: 2055 64X8 MNOS ROM	30E
75	YY000253	8	230027	IC: 8264 - 64K RAM	22D THRU 29D
76	YY011308	1	230028	IC: Z80A SIO/O	24F
77	YY005930	1	230029	IC: Z80A CTC CNTRL CRCT	21F
78	YY005930	2	230034	IC: M58725P 2K X 8 RAM	16C, 16D

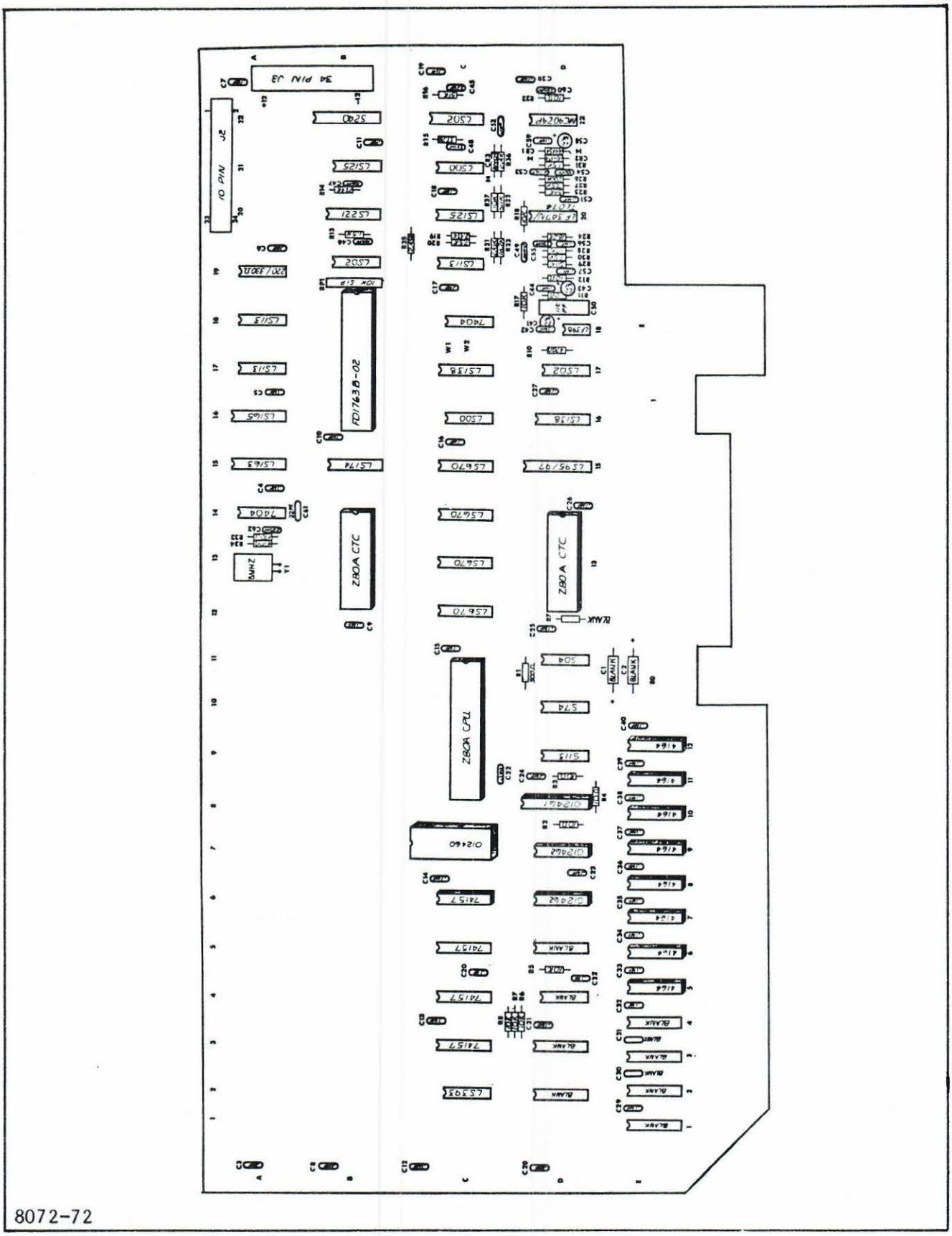

Figure 6-9. Advanced Floppy Disk Controller Circuit Board Assembly Diagram AFC

Table 6-9. Advanced Floppy Controller Parts List (Used on S/10 System)
TT520060, P/N 051301

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
1	YY003794	1	130008	CRYSTAL: 8MHZ PC SOLDER	Y1
2	YY010797	3	151010	CAP: 100 PF 50V	C46, C47, C54
3	YY011310	1	151020	CAP: .001 MF CERAMIC DIP, 40V	C53
4	YY010754	45	151040	CAP: .1 MF 50V	C1 THRU C29, C42, C44, C51, C52, C57, C56, C59, C32 THRU C40
5	YY010798	1	152200	CAP: 22 PF 50V	C61
6	YY010799	2	152210	CAP: 220 PF 50V	C60, C62
7	YY010800	4	152262	CAP: 22MF GUMDROP ELEC, 15V	C41, C43, C45, C58
8	YY006794	2	153311	CAP: 330 PF SILVERMICA 5%	C55, C48
9	YY011311	1	154701	CAP: 0047 MFZ 1000V + 10%	C49
10	YY010779	1	230001	IC: 81LS95/97 OCTL BUFF	15D
11	YY010934	1	230019	IC: 96LS02 DUAL LS RET/RSS	22C
12	YY011312	1	230030	IC: LF374N/TL074 OP AMP	20D
13	YY011313	1	230031	IC: LF398 SMP/HOLD AMP	18D
14	YY003525	1	230032	IC: MC4024P VCO	22D
15	YY000439	2	231004	IC: 74LS04 HEX INVTR	14A, 18C

Table 6-9. Advanced Floppy Controller Parts List (Used on S/10 System) TT520060, P/N 051301 (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
16	YY000162	4	231157	IC: 74157 QUAD 2 TO 1	3C THRU 6C
17	YY000438	2	232000	IC: DM74LS00 QD 2-INP + NG	16C, 21C
18	YY999390	2	232002	IC: NPN 74LS02	17D, 19B
19	YY002688	3	232113	IC: 74LS113 DUAL JK FLIP-FLOP	17A, 18A, 19C
20	YY003583	2	232125	IC: 74LS125 QD BUSBUF 3OUPT	20C, 21B
21	YY003585	2	232138	IC: 74LS138 3 TO 8 DCDR MUX	16D, 17C
22	YY005908	1	232163	IC: 74LS163 4BIT BIN CTR	15A
23	YY010935	1	232165	IC: 74LS165 PAR 8BIT SHT RG	16A
24	YY000446	1	232174	IC: 74LS174 HEX D FLIP-FLOP	15B
25	YY002611	1	232221	IC: 74LS221 DUAL MONO MULT	20B
26	YY010933	1	232393	IC: 74LS393 DUAL 4BIT BIN CTR	2C
27	YY006539	4	232670	IC: 74LS670 4X4 RGTR FILES	12C THRU 15C
28	YY000027	1	233004	IC: 74S04 HEX INVERTERS	11D
29	YY000746	1	233074	IC: 74S74 DUAL D + TRIG F/F	10D
30	YY004252	1	233113	IC: 74S113 DUAL JK TRIG F/F	9D
31	YY000044	1	233240	IC: 74S240 OCT BUF L DR/REC	22B
32	YY010939	2	270001	R: 18.2K OHM 1% 1/4W M/FL	R23, R24
33	YY010940	1	270002	R: 27.4K OHM 1% 1/4W M/FL	R14
34	YY010941	3	270003	R: 2.43K OHM 1% 1/4W M/FL	R19, R21, R35

Table 6-9. Advanced Floppy Controller Parts List (Used on S/10 System) TT520060, P/N 051301 (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
35	YY010937	1	270004	R: 33.2K OHM 1% 1/4W M/FL	R15
36	YY010944	4	270005	R: 10K OHM 1% 1/4W M/FL	R17,R18,R28,R37
37	YY010938	2	270006	R: 7.5K OHM 1% 1/4W M/FL	R20, R27
38	YY009519	3	270007	R: 511K OHM 1% 1/4W M/FL	R22, R25, R29
39	YY010945	1	270008	R: 200K OHM 1% 1/4W M/FL	R26
40	YY011314	3	270009	R: 1.5K OHM 1% 1/4W CC	R30. R31. R13
41	YY011335	1	270012	R: 220/330 OHM NETWORK	19A
42	YY007837	1	270013	R: 51K OHM 1% 1/4W M/F	R16
43	YY007852	6	271000	R: 10 OHM 5% 1/4W	R2, R3, R4, R11 R12, R32
44	YY000130	4	271030	R: 10K OHM 5% 1/4W CC	R5 THRU R8
45	YY010749	1	271032	R: NETWORK 10K SIP	RP1
46	YY010750	1	272420	R: 2.4K OHM 5% 1/4W CC	R36
47	YY000119	1	273010	R: 300 OHM 5% 1/4W CC	R1
48	YY000067	3	274710	R: 470 OHM 5% 1/4W CC	R33, R34, R10
49	YY000187	3	284454	DIODE: 1N4454	CR1, CR2, CR3
50	YY011315	1	012460	EPROM: MPM 2716	7C
51	YY011316	1	012461	IC: DMPAL 16R6CJ MEMORY CNTRLR AFC	8D

Table 6-9. Advanced Floppy Controller Parts List (Used on S/10 System) TT520060, P/N 051301 (continued)

ID	ICN	QTY	PART NUMBER	DESCRIPTION	LOCATION
52	YY005931	1	230011	IC: Z80 MICRO PROC CPU	9C
53	YY010962	1	230021	IC: FD1763 B02 TR DAT BUF	17B
54	YY011317	8	230024	IC: 16 X 1 RAM M5K4164ANS	5E THRU 12E
55	YY005930	2	230029	IC: Z80A CTC CNTRL CRCT	13B, 13D
56	YY011334	2	012462	IC: AFC CONTROLLER 74S287	6D,7D
57	YY011318	1	151130	CAP: MIAL 12000H POLYSTYRENE	C50

Table 6-10. S/10 Power Supply Parts List Phase 1B, TT527010 P/N 200008

ID	ICN	DESCRIPTION	LOCATION
01	YY000643	RES 3.6K 1/4W 5% CAR FILM	R101
02	YY000731	RES 15 OHMS 1/4W 5% CAR FILM	R102
03	YY000068	RES 1K 1/4W 5% CAR FILM	R131, R103, R111, R115, R116
04	YY000058	RES 10 OHMS 1/4W 5% CAR FILM	R104
05	YY000061	RES 82 OHMS 1/4W 5% CAR FILM	R105
06	YY000118	RES 220 OHMS 1/4W 5% CAR FILM	R107
07	YY005721	POT 2K	R108, R127
08	YY000117	RES 150 OHMS 1/4W 5% CAR FILM	R109, R110, R112
09	YY000062	RES 100 OHMS 1/4W 5% CAR FILM	R113, R114, R117, R118, R119
10	YY011407	RES 1 OHM 1/4W 5% CAR FILM	R120
11	YY007135	RES 33 OHMS 2W 5% METAL FILM	R121
12	YY006966	RES 240K 1/2W 5% CAR FILM	R122, R123
13	YY006956	RES 27K 1/2W 5% CAR FILM	R124
14	YY007440	POT 100K	R125
15	YY005606	RES 62 OHMS 1W 5% CAR FILM	R126
16	YY011571	RES 1.3 OHMS 1/2W 5% CAR FILM	R128
17	YY006973	RES 470K 1/2W 5% CAR FILM	R129
18	OT001295	RES 1.2K 1/4W 5% CAR FILM	R130

Table 6-10. S/10 Power Supply Parts List Phase 1B, TT527010 P/N 200008 (continued)

ID	ICN	DESCRIPTION	LOCATION
19	YY006935	RES 75 OHMS 1/2W 5% CAR FILM	R132
20	YY005397	CAP 2.2MF 15V TANT	C101
21	YY000668	CAP 2200MF 10-16V ALUM ELECT	C102
22	YY008119	CAP 220MF 25V ALUM ELECT	C103, C104, C122, C123
23	YY011410	CAP 330MF 16V ALUM ELECT	C105, C109
24	YY011411	CAP 1000MF 10V ALUM ELECT	C106, C107, C108, C124
25	YY011412	CAP .0047MF 3KV DISC CER	C110
26	YY011413	CAP 100MF 200V ALUM ELECT	C111, C112 - C114
27	YY011447	CAP .0047MF 600V DISC CER	C115
28	YY006783	CAP .1MF 400V ORANGE DROP	C116
29	YY011409	CAP 2.2MF 16V TANT	C117
30	YY007486	CAP 33MF 10V TANT	C118
31	YY000207	CAP 1MF 25V DISC CER	C119
32	YY005416	CAP .01MF 100V MYLAR	C120
33	YY011448	CAP 330MF 35V ALUM ELECT	C121
34	YY011449	DIODE 1N4743 ZENER	D101
35	YY009644	DIODE 1N4733 ZENER	D102

Table 6-10. S/10 Power Supply Parts List Phase 1B, TT527010 P/N 200008 (continued)

ID	ICN	DESCRIPTION	LOCATION
36	YY002992	DIODE MR821	D103, D118
37	YY011450	DIODE 80SQ035	D104
38	OA041400	DIODE 1N4004	D105, D108, D111, D117, D119
39	YY004802	DIODE MR851	D109, D116
40	YY005760	DIODE 1N4936	D110
41	YY011415	DIODE 1N988	D112, D113
42	YY000352	DIODE 1N914	D114, D115
43	YY005789	IC V/RG 7905	A101
44	YY000461	SCR C122F	A102
45	YY002618	TRANS 4N25 OPTO	A103
46	YY005784	LM317K	A104
47	YY011444	INDUCTOR 155-5601	L101, L103, L104
48	YY011445	INDUCTOR #065	L102, L105
49	YY000767	TRANS 2N3904 NPN	Q101, Q102
50	YY000768	TRANS 2N3906 NPN	Q103
51	OD900013	TRANS 2N2219 NPN	Q104
52	YY011416	TRANS 2N4871	Q105
53	YY011572	TRANS 2N6545	Q106

Table 6-11. ODT Power Supply Parts List Phase 1B, TT527020 P/N 200007

ID	ICN	DESCRIPTION	LOCATION
01	YY000643	RES 3.6K 1/4W 5% CAR FILM	R103
02	YY000731	RES 150 OHMS 1/4W 5% CAR FILM	R102
03	YY000058	RES 10 OHMS 1/4W 5% CAR FILM	R104
04	YY000061	RES 82 OHMS 1/4W 5% CAR FILM	R104
05	YY000068	RES 1K 1/4W 5% CAR FILM	R106, R111, R115, R116
06	YY000062	RES 100 OHMS 1/4W 5% CAR FILM	R113, R114, R117, R118
07	YY000119	RES 300 OHMS 1/4W 5% CAR FILM	R119
08	YY000117	RES 150 OHMS 1/4W 5% CAR FILM	R109, R110, R112
09	YY011407	RES 1 OHM 1/4W 5% CAR FILM	R120
10	YY007135	RES 33 OHMS 2W CAR FILM	R121
11	YY006966	RES 240K 1/2W 5% CAR FILM	R122, R123
12	YY006960	RES 56K 1/2W 5% CAR FILM	R124
13	YY007440	POT 100K	R125
14	YY005384	RES 39 OHMS 1W 5% CAR FILM	R126, R132
15	YY005721	POT 2K	R127
16	YY011408	RES 1.6 OHMS 1/2W 5% CAR FILM	R128
17	YY006973	RES 470K 1/2W 5% CAR FILM	R129

Table 6-11. ODT Power Supply Parts List Phase 1B, TT527020 P/N 200007 (continued)

ID#:	ICN:	DESCRIPTION:	LOCATION:
18	YY011409	CAP 2.2MF 16V SOLID TANTALUM	C101, C117
19	YY000668	CAP 2200MF 16V ALUM ELECT	C102
20	YY008119	CAP 220MF 25V ALUM ELECT	C103, C014, C122, C123
21	YY011410	CAP 330MF 16V ALUM ELECT	C105, C109
22	YY011411	CAP 1000MF 10V ALUM ELECT	C106, C107
23	YY011412	CAP .0047MF 3KV DISC CER	C110
24	YY011413	CAP 100MF 200V ALUM ELECT	C111, C112, C113, C114
25	YY011311	CAP .0047MF 1000V	C115
26	YY006783	CAP 1MF 400V ORANGE DROP	C116
27	YY007706	CAP 33MF 10V 5% TANT	C118
28	YY000207	CAP .1MF 25V DISC CER	C119
29	YY005416	CAP .01MF 100V MYLAR	C120
30	YY005789	IC V/RG 7905	A101
31	YY000461	C122F	A102
32	YY002618	4N25	A103

Table 6-11. ODT Power Supply Parts List Phase 1B, TT527020 P/N 200007 (continued)

ID#:	ICN:	DESCRIPTION:	LOCATION:
33	YY009644	DIODE 1N4733	D102
34	YY002992	DIODE MR821	D103
35	YY011414	DIODE ECR81004	D104
36	OA041400	DIODE 1N4004	D105, D106-D108, D111
37	YY004802	DIODE MR851	D109
38	YY005760	DIODE 1N4936	D110
39	YY011415	DIODE 1N988	D112, D113
40	YY000352	DIODE 1N914	D114
41	YY011444	INDUCTOR 155-5601	L101, L103
42	YY011445	UNDUCTOR 065	L102
43	YY000767	TRANS 2N3904	Q101, Q102
44	YY000768	TRANS 2N3906	Q103
45	OD900013	TRANS 2N2219	Q104
46	YY011416	TRANS 2N4871	Q105
47	YY011417	TRANS SJ6942	Q106

Table 6-12. Motherboard Parts List TT520040 P/N 051131 (Phase 1B)

ID#:	ICN:	DESCRIPTION:	VPN:	QTY:	LOCATION:
01	OT000314	RES 470 OHMS 1/2W 5%	274711	1	R1
02	OT000382	RES 910 OHMS 1/4W 5%	279110	1	R2
03	YY000350	TRANS 2N3645 PNP	283645	1	Q1
04	YY000767	TRANS 2N3904	283904	1	Q2
05	YY000187	DIODE 1N4454	284454	1	CR1

SECTION VII

5.25" FIXED DISK DRIVE

7.1 INTRODUCTION

This section provides maintenance personnel with information necessary to install, operate, and maintain the 5.25" Fixed Disk Drive.

This section is arranged in four subsections. The scope of each subsection is described as follows:

7.1 INTRODUCTION, contains general information, physical and electrical descriptions, and equipment specifications.

7.2 INSTALLATION and OPERATION, contains information to enable maintenance personnel to inspect and install the Disk Drive and Controller. Preliminary checks are also included. This subsection also explains and shows the location and use of status and fault isolation indicators, as well as power-up and power-down procedures.

7.3 FUNCTIONAL DESCRIPTION, explains the drive and controller operations and gives a detailed description of each function. Simplified logic and block diagrams, timing diagrams, and waveforms are included.

7.4 MAINTENANCE, contains corrective maintenance procedures.

7.5 REMOVAL and REPLACEMENT PROCEDURES, describes sequence and step-by-step procedure in removing major subassemblies.

7.6 PARTS LIST

7.1.1 General Description

The disk drives are fixed-media, random-access, rotating memory storage devices that enable the central processing unit (CPU) of a data processing system to store and retrieve blocks (records) of data on rotating disks. The drive functions as the input/output device for the CPU.

There are two disk drives in the series containing 2 or 4 magnetic disks which range in total data storage from 13.33 megabytes to 26.67 megabytes, unformatted, and 10.49 megabytes to 20.97 megabytes, formatted. Access to data is provided by one moving head per disk surface. The heads are an integral part of the head disk assembly (HDA) and never require alignment in the field. Data is recorded on the disk surface using modified frequency modulation (MFM) techniques.

The drive incorporates an open-loop, stepper-motor-type positioning system. The major components of the drive are illustrated in figure 7-1 and are explained in the following paragraphs.

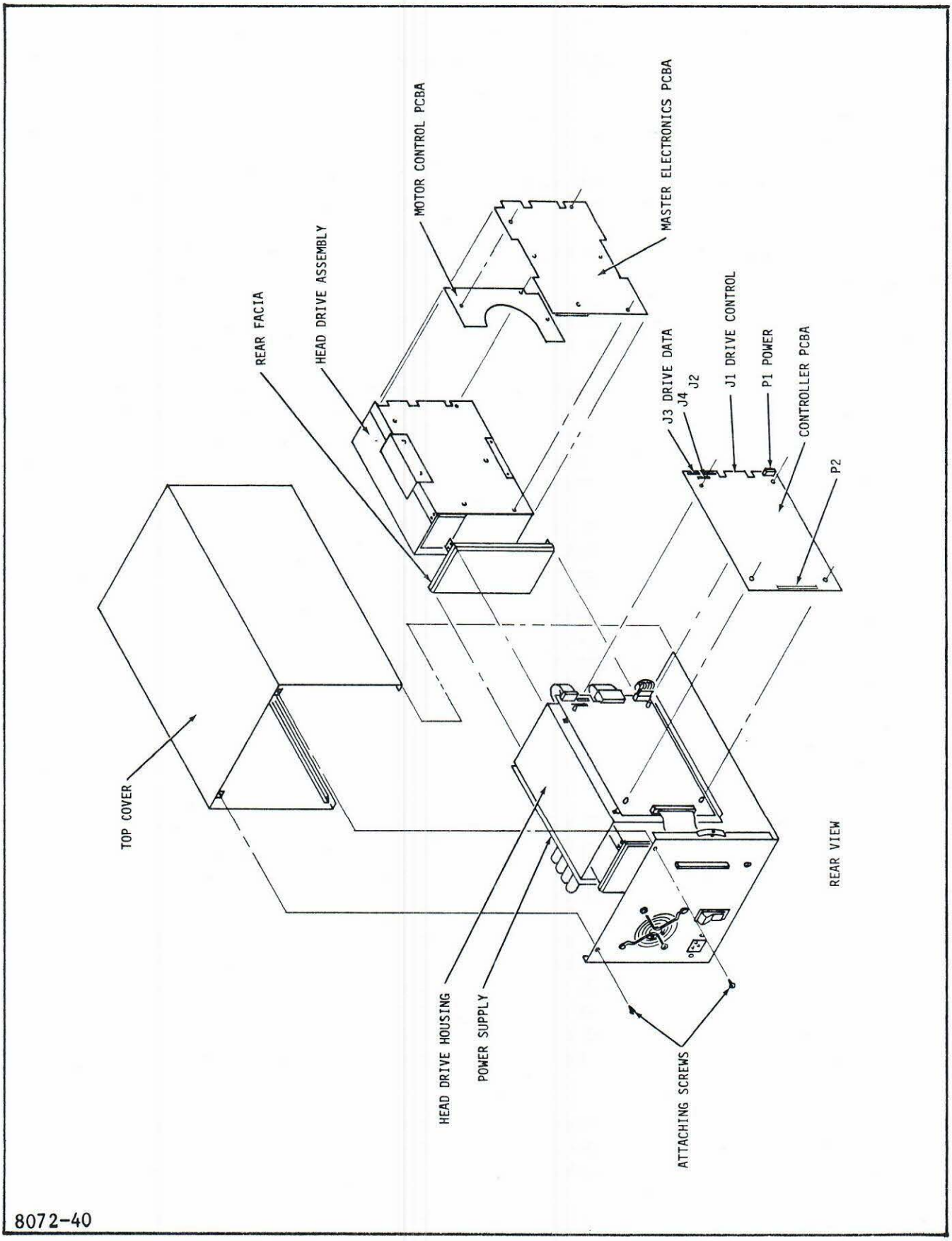

Figure 7-1. Major Component Location

Head Disk Assembly - The head disk assembly, shown in figure 7-2, is a completely sealed module that houses the read/write heads, disks, positioner assembly, stepper motor, and filters. The spindle-mounted disks are rotated by the dc motor as the read/write heads fly over the surface of the disk. The stepper motor positions the heads over the disk, using positioning information from a microprocessor. Within the sealed module, the airflow generated by disk rotation causes air to flow from the disk chamber (upper chamber) through an aperature into the drive chamber (lower chamber) and to return via a recirculating filter.

DC Motor and Brake - The dc motor is a brushless, two-phase external rotor motor with integral hub and commutation effected by a Hall sensor. The rotational speed of the motor is 3600 revolutions per minute (rpm). The disk hub is grounded to the master electronics board via the motor shaft and a button contact. The brake is a plunger-solenoid designed to stop the motor in five seconds and to provide a restraining torque during handling.

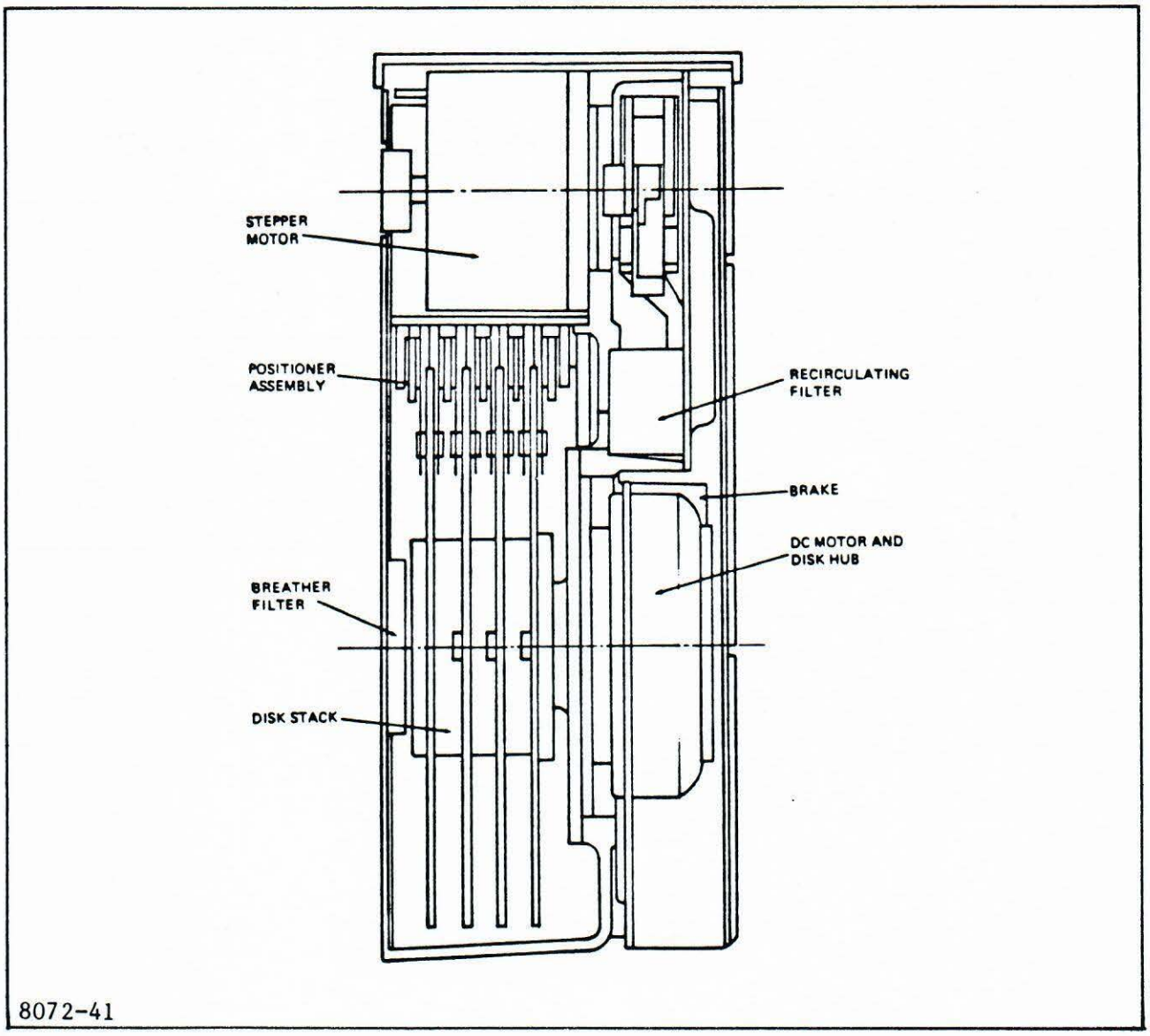

Figure 7-2. Head Disk Assembly

Disk Electronics - The Disk electronics consist of four standard printed circuit board assemblies (PCBAs); Master Electronics, Preamplifier Board, Motor Control Board, and Disk Controller Board.

Power Supply - The dc supply voltages (+12 and +5 volts) to the disk drive are supplied by the Disk Power Supply and input to the drive on connector J3.

7.1.2 Functional Concept

The simplified block diagram in figure 7-3 shows the functional concept of the disk drive. Additional detailed explanations of the logic areas are discussed in paragraph 7.3.

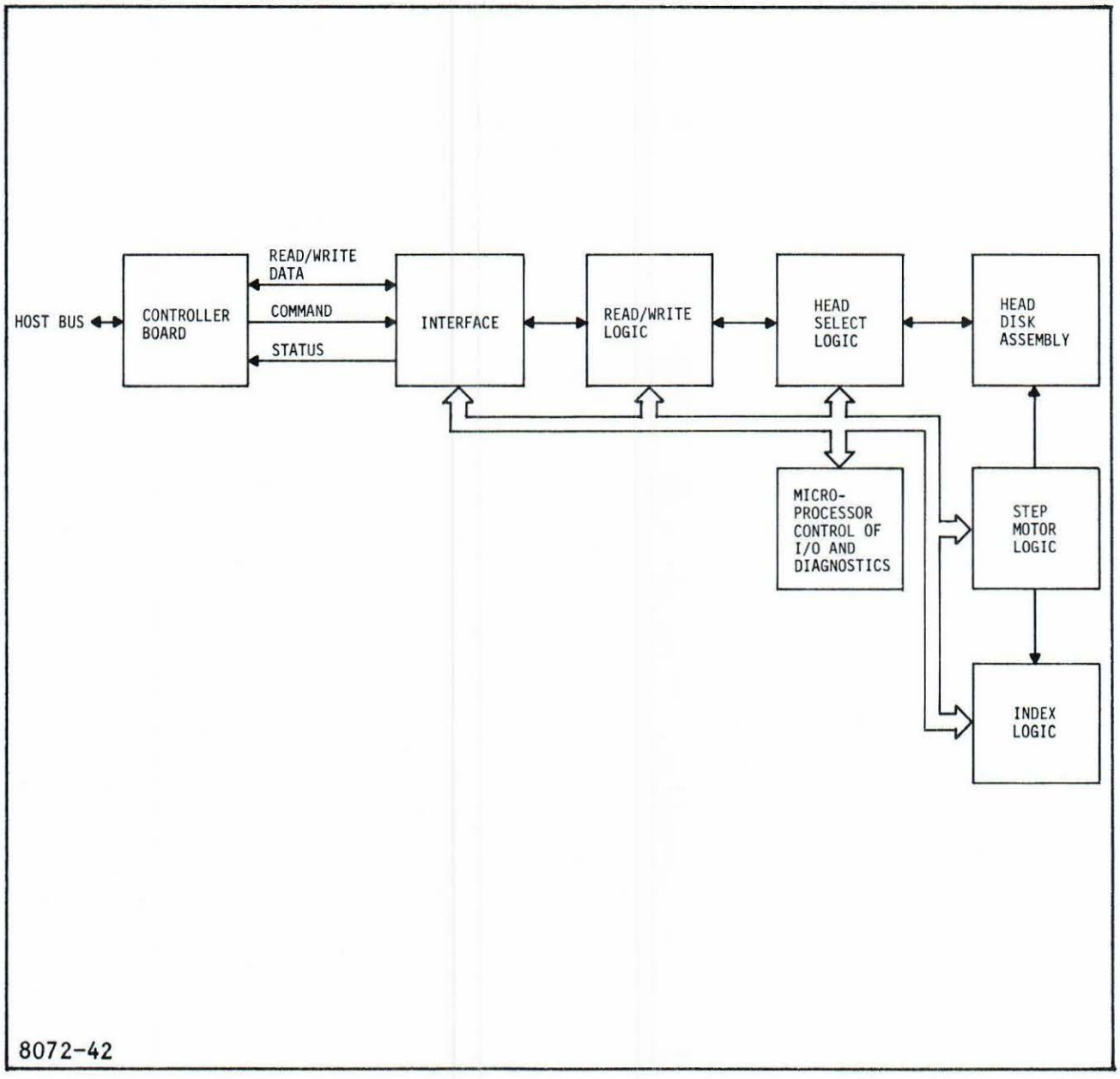

Figure 7-3. Simplified Block Diagram

Interface Logic - The interface logic translates the input/output signals of the disk drive to ensure drive-to-controller signal compatibility. Disk drive logic signal levels are transistor-to-transistor logic (TTL) compatible. The transmission line signals are differential signals.

Read/Write Logic - To execute read or write commands, the drive must be free of faults and the selected head must be at the correct location on the disk (i.e., on cylinder). During a read command, the read/write logic recovers data from the disk, processes the data, and transfers the data to the controller. During a write command, the read/write logic receives data from the controller, processes the data and writes it on the disk.

Head Select Logic - The head select logic receives and decodes the addresses of a specific head.

Step Motor Logic - A four-phase stepper motor is used to control the read/write heads in the proper sequence at a rate and direction determined by a microprocessor.

Index Logic - The square wave output of the Hall sensor in the dc motor is processed to produce a pulse every disk revolution. This pulse is used as an interface signal to mark a fixed reference point relative to the disk.

Disk Controller - The Disk Controller uses the Shugart Associates System Interface (SASI). It does not require special considerations in order to communicate with the host bus. Operating features of the Controller are: Interlocked data transfer through SASI; Microprocessor based architecture; Full-sector buffer (256 bytes); Automatic retries during disk access; Internal Diagnostics and Variable Interleave.

7.1.3 Equipment Specifications

Performance characteristics for the Disk Drive are listed in table 7-1.

Table 7-1. Specifications

PARAMETERS	CHARACTERISTIC	
	10 Megabyte	20 Megabyte
Storage capacity (Unformatted)		
Disks per drive	2	4
Cylinders	320	320
Tracks per cylinder	4	8
Data bytes per track	10,417	10,417
Tracks per drive	1280	2560
Capacity (megabytes)	13.33	26.67

Table 7-1. Specifications (continued)

PARAMETERS	CHARACTERISTIC	
	10 Megabyte	20 Megabyte
Storage capacity (Formatted)		
Data bytes per sector	256	256
Data sectors per track	32	32
Data bytes per track	8192	8192
Capacity (megabytes)	10.49	20.97
Recording parameters		
Bit density	8900 bpi (inner track, nominal)	
Coding	Modified-frequency-modulation (MFM)	
Track density	360 tracks per inch (average)	
Rotational parameters		
Disk rotational speed	3600 (± 1%) rpm	
Data transfer rate	5 Mbits per second	
Cylinder access time		
Ramp mode		
Single cyllinder	18 milliseconds (average)	
320 cylinders	215 milliseconds (maximum)	
Cylinder access	90 milliseconds (average)	
3 milliseconds step mode		
Single cylinder	18 milliseconds (average)	
320 cylinders	1035 milliseconds (maximum)	
Cylinder access	360 milliseconds (average)	
Slow pulse mode*		
Single cylinder	23 milliseconds (average)	
320 cylinders	step rate=pulse rate	
Cylinder access	step rate=pulse rate (average)	
Data access time		
Average latency	8.3 milliseconds	
Average data access time/ramp mode	98.3 milliseconds	
Average data access time/3 milliseconds step mode	368.3 milliseconds	
Head switching time	8 microseconds (maximum)	

*This option requires the removal of jumper A from pin 14 of the microprocessor on the master electronics board.

Table 7-1. Specifications (continued)

PARAMETERS	CHARACTERISTIC
Error rates (These error rates are valid only when the drive is used according to specification. Media defects or equipment failures are excluded. Written data should be verified as being correctly written. All media defects should be flagged.)	
Seek errors	1 in 10^6 seeks
Recoverable read errors	1 in 10^{10} bits
Nonrecoverable read errors	1 in 10^{12} bits

STORAGE	TRANSIT	OPERATING
Temperature: -40°F to 158°F -40°C to 70°C	-40°F to 158°F -40°C to 70°C	50°F to 122°F 10°C to 50°C
Temperature Gradient: 27°F per hour 15°C per hour	20°F per hour 15°C per hour	18°F per hour 10°C per hour
Humidity: 5-90% RH no condensation	5-90% RH no condensation	10-85% RH no condensation
Humidity Gradient: 20% per hour	20% per hour	20% per hour
Altitude: -1000 to +40,000 ft.	0 to +40,000 ft.	-1000 to +10,000 ft
Vibration: 0.2 in. pk. to pk. displacement (5 Hz to 20 Hz)	0.2 in. pk. to pk. displacement (5 Hz to 20 Hz)	0.006 in. pk. to pk. displacement (5 Hz to 60 Hz)
Shock: Withstand drop of 36 inches	Withstand drop of 36 inches	3.0g peak 10 milliseconds duration, 2 shocks/sec, max.
RF Interference:		1 volt/meter rms (1.5 Hz - 10GHz)

Table 7-1. Specifications (continued)

PARAMETERS	CHARACTERISTIC	
STORAGE	TRANSIT	OPERATING
Magnetic field:		0.0003 tesla. max.
Emitted Acoustic Noise:		54 db, max., (continuous)
DISK CONTROLLER BOARD		
VOLTAGE	RANGE	CURRENT
+5.0 Vdc	4.75 to 5.25	2.5 Amps max.
+12.0 Vdc	10.8 to 13.2	66.0 ma max.

7.2 INSTALLATION AND OPERATION

This subsection contains unpacking, installation, and checkout information for the 10 or 20 megabyte Disk Drive.

7.2.1 Unpacking

Prior to unpacking the drive, inspect the packaged drive to determine whether any damage has been incurred during shipment.

1. Using the shipping documents, verify that all items have been received.
2. Open protective shipping carton at top.
3. Remove drive from shipping carton.
4. Remove plastic cover.
5. Inspect each package article to determine whether any damage has been incurred during shipment.
6. Verify that connectors, indicators, and protruding parts are undamaged.
7. Check ID nameplate against shipping papers to verify that drive part number and serial number are correct.
8. When practical, store shipping containers for reuse.
9. Record any damage, and report damage to the applicable carrier.

7.2.2 Equipment Placement

Equipment placement consists of mounting the drive, routing the input/output cables and grounding the equipment.

7.2.3 Shipping Lock (Read/Write Heads)

The stepper motor lock is fixed in place automatically through a relay. The lock prevents movement of the read/write heads across the disk surfaces during shipment or other movement.

7.2.4 Step Rate Selection

The disk drive has a step rate operational range of 10 microseconds to 8 milliseconds. This operational range has three bands; two ranges are automatically selected by the microprocessor, and one is selected by removing Link A on the master electronics board.

Link A in: step rate 10 microseconds to 200 microseconds
Link B in: step rate 700 microseconds to 3.1 milliseconds
Link A out: step rate 3.1 milliseconds to 8.0 milliseconds

7.2.5 System Installation

Installation of the Disk Drive consists of routing the Interface cable to the System S/10 and connection of the Interface Board on the Advanced Floppy Controller board.

All components required to interface the 5.25" Disk Drive to the System S/10 are included. The following is a list of all the interface components and part numbers.

Interface Circuit Board (PCBA)	903370-001
Ribbon Cable	906608-011
Cable Clamp Bracket	907363-001
Cable Clamp Bracket Plate	907364-001

Interface Cable Pin Assignment - The cable connectors required are standard-insulation, displacement type connectors designed for use with flat-ribbon cables. Table 7-2 lists the connector pin assignment for the interface cable.

Table 7-2. Interface Cable Pin Assignment

SIGNAL PIN	GROUND RETURN	SIGNAL NAME
2	1	DATA0-
4	3	DATA1-
6	5	DATA2-
8	7	DATA3-
10	9	DATA4-
12	11	DATA5-
14	13	DATA6-
16	15	DATA7-
18	17	Spare
20	19	Spare
22	21	Spare
24	23	Spare
26	25	Spare
28	27	Spare
30	29	Spare
32	31	Spare
34	33	Spare
36	35	BUSY-
38	37	ACK-
40	39	RST-
42	41	MSG-
44	43	SEL-
46	45	C-/D
48	47	REQ-
50	49	I-/O-

Cable Routing and Interface Connection - Cable routing and connection of the interface board should be installed in accordance with the following procedure. Figures 7-4 through 7-6 provide illustrative views for installation.

1. Remove AC power cord and port connectors from the rear of the S/10.

2. Rotate the S/10 cabinet cover latch fully clockwise. Using a flat, non-metal tool, snap open the top cover.

3. Remove the power connector and logic connector located on the right side of the Floppy Controller board.

4. Remove both the Video Processor board and the Floppy Controller board (refer to paragraph 5.2).

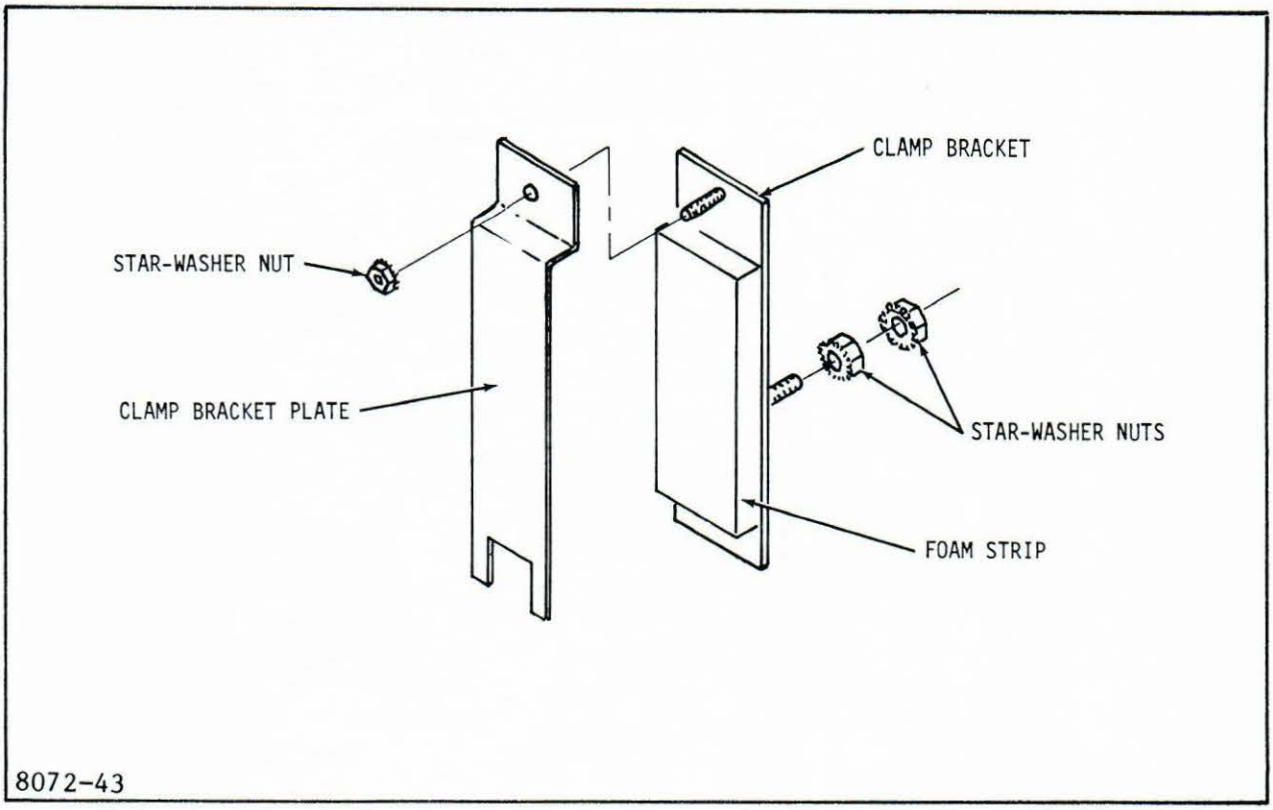

Figure 7-4. Cable Clamp Bracket and Plate

6. Mount the cable clamp bracket on the inside of the housing as shown in figure 7-5. The threaded stud on the bracket is inserted through the screen and second vent slot on the left side of the housing. It will be necessary to puncture a hole in the metalic screen to insert the bracket stud. Attach a starwasher nut to secure the clamp bracket in place.

7. Insert the unshielded side of the flat ribbon cable through the AUX port hole in the cabinet. When inserting the ribbon cable ensure that the red strip side of the cable is down (bottom side). See figure 7-6.

8. Fold and route the ribbon cable as shown in figure 7-6. The red strip should be on the top side where connection is made to the interface board.

9. Attach the cable to the clamp bracket with the clamp plate and star-washer nut. Attach ribbon cable ground wire to clamp bracket stud with star-washer nut. See figure 7-5.

10. Remove the Z80A from the Advanced Floppy Controller PCBA. Return Z80A to stock.

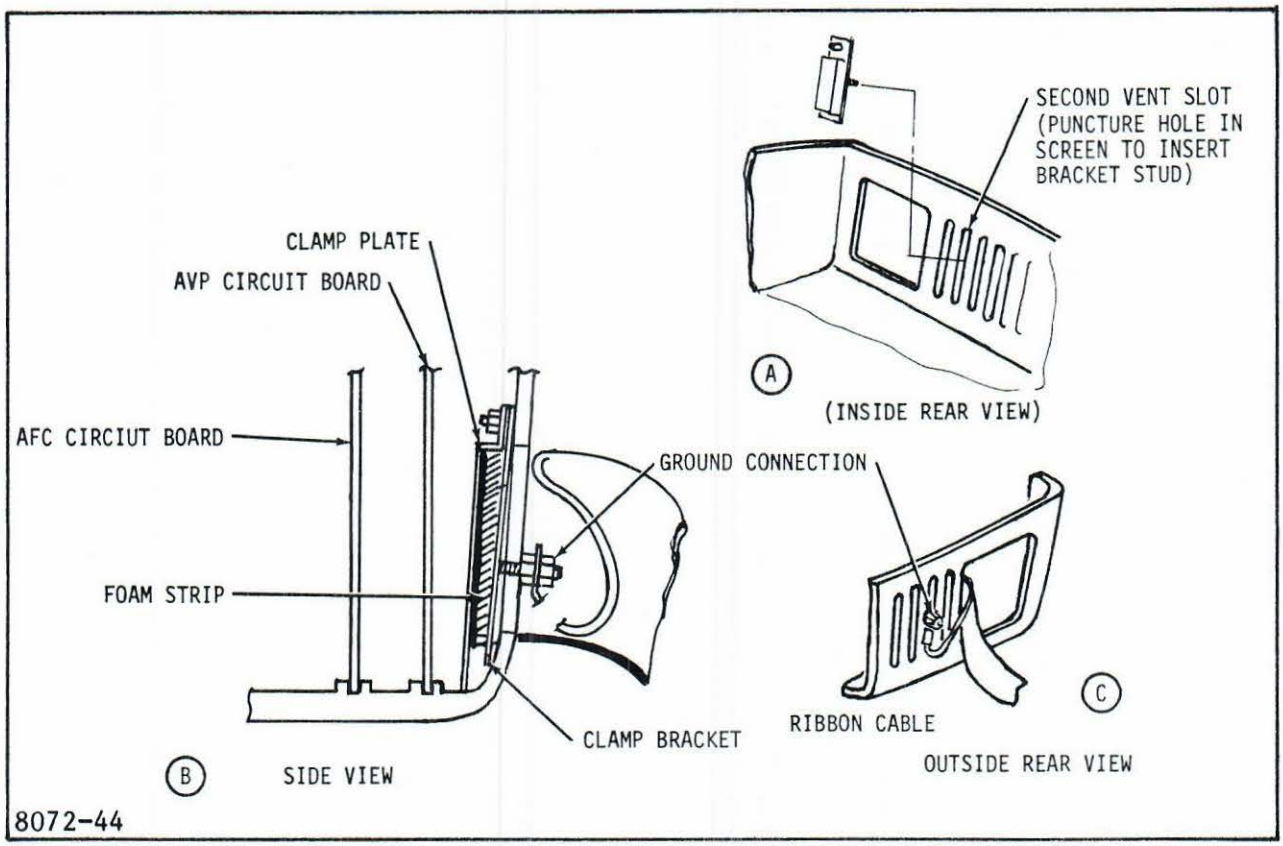

Figure 7-5. Cable Clamp Bracket Installation

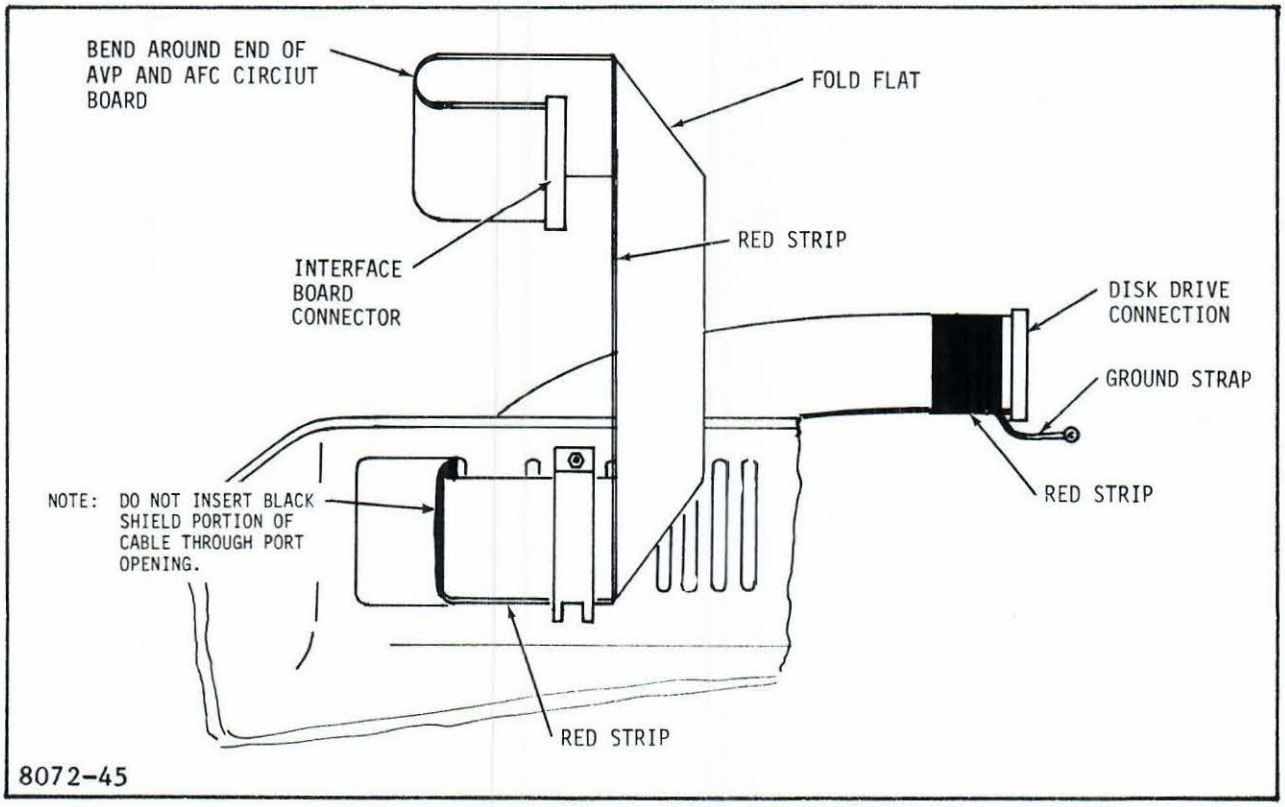

Figure 7-6. Cable Routing and Fold

11. Loosen PCBA mounting bracket screws to allow connector to be plugged into Z80 socket. Plug the Interface PCBA (903370-001) into the Z80 socket on the Advanced Floppy Controller PCBA. Tighten the Interface PCBA mounting bracket screw. See figurej 7-7.

12. Reinstall the ADVANCED VIDEO Processor PCBA and Advanced Floppy Controller PCBA. (Refer to paragraph 5.2). Replace all cables removed in number 3.

13. Connect the other end of ribbon cable to the Disk Drive Assembly. Attach ribbon cable ground wire to connector screw.

14. Run "S/10 Hard Disk Diagnostic Program" (Doc. No. 011159).

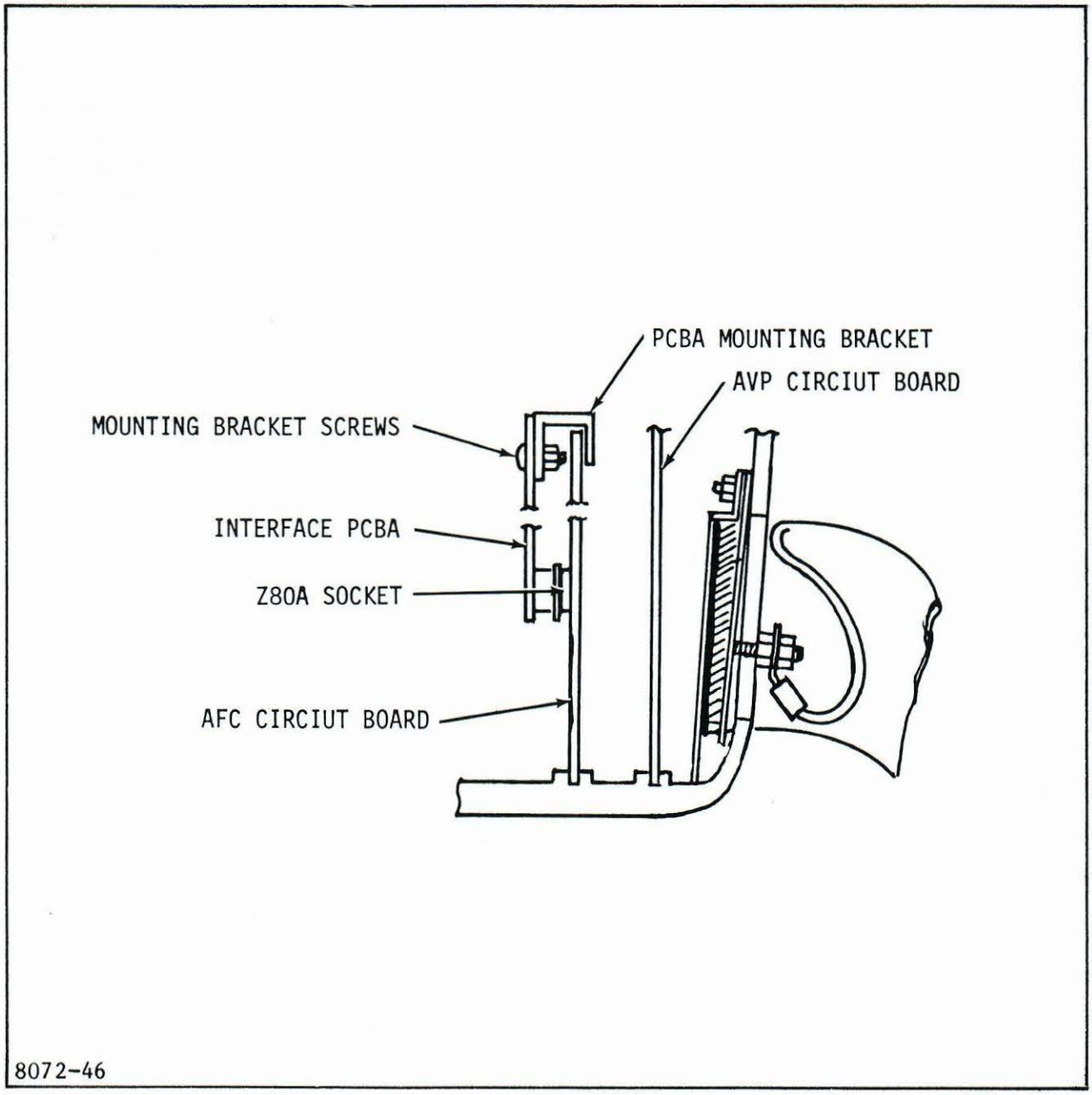

Figure 7-7. Interface PCBA and Bracket Mounting

7.2.6 Operation

Operating instructions consist of indicator functions, power-on/off procedures and voltage checks.

Indicators - When lit, the two red LEDs fixed to the master electronics board are visible through the facia. The Power On LED is located closest to the center of the facia and is on when the drive is Ready and no error is present. It is also used to indicate fault conditions in the drive (table 7-3).

The Power On LED will not come on, indicating an error, if +5 volt supply does not come up and stabilize within one second. (The microprocessor does not receive an initial reset.)

The Select On LED comes on (provided the Power On LED is on) when the drive is ready and selected by the host.

Power-On Procedures - The Disk Drive requires +12 volts and +5 volts dc source power, and these voltages are measured at drive connector J3. At power-on, the drive motor takes 4 amperes at +12 volts, dropping to 2.4 amperes (maximum) after 10 seconds. For power-up or power-down sequences, the +12 volt and +5 volt supplies may be applied or removed in any order. However, if the +5 volt power is applied first, the +12 volt should follow within 5 seconds or the fault detection circuitry will issue an error indication.

On power-up, the drive performs an automatic re-calibration sequence which includes a disk speed check, accurate to $\pm$1% of nominal, a seek to track 000 and an index pulse selection. The host uses status Ready to sense the completion of this sequence. The time until Ready turns true varies for each model of the Disk Drive. Maximum times are as follows:

MODEL	TIME TO READY
10 Megabyte	10 seconds
20 Megabyte	18 seconds

Table 7-3. Diagnostic and Failure Code Indicators

ACTION	ABNORMAL RESULT (DOT - DASH CODE)	RESULT
Power-Up drive		LED flashes at 0.5 seconds intervals After 25 seconds maximum, LED stops flashing and remains on. Heads are at track 0
Code 1	LED displays* . . . -	No index track data burst at track-2 or track-3
Code 2	LED displays . . - .	No flag 0 from track 0 detector
Code 3	LED displays . . - -	Motor speed exceeds ±1% tolerance during normal operation
Code 4	LED displays . - . .	Motor speed exceeds +10%, -5% tolerance during normal operation
Code 5	LED displays . - . -	Flag 0 always true
Code 6	LED displays . - - .	Step pulse while Write Gate true
Code 7	LED displays . - - -	Static write fault condition **
Code 8	N/A	
Code 9	LED displays - . . -	Microprocessor self-test failed
Code 10	LED displays - . - .	No Index
Code 11	LED displays - . - - LED remains OFF LED remains ON LED flashes (erratic)	Motor not up to speed Firmware/microprocessor fault Firmware/microprocessor fault Firmware/microprocessor fault
Code 12	LED displays - - . .	Found index track data burst, but cannot set index

*For the fault codes, a four-bit binary code is used. Long flash (-) = logic 1, a short flash (.) = logic 0, with the most significant bit (MSB) occuring first.

**Write Fault Conditions:

1. Write current and no Write Gate
2. No write current and Write Gate
3. More than one read/write head selected
4. 12-volt supply drops below 10.3 volts
5. 5-volt supply drops below 4.5 volts

Power Supply Checks - The following loads are used to check the power supplies. For the 12-volt supply, the power-up current is measured using a standard load of 3 ohms in parallel with 1 millihenry and the operating current is measured using 5 ohms in parallel with 1 millihenry. With a 7-ohm resistive load on the 5-volt supply and the aforementioned loads on the 12-volt supply, noise and ripple should be no more than 100 millivolts peak-to-peak up to 500 hertz and 50 millivolts peak-to-peak from 500 hertz to 5 megahertz.

The power requirements of the Disk Drive are listed in table 7-4.

Table 7-4. Power Requirements

VOLTAGE (VDC)	TOLERANCE	CURRENT NOMINAL	CURRENT MAXIMUM
+ 5	± 5%	0.65A	0.75A
+12	±10%	2.0 A	2.4 A

7.3 FUNCTIONAL DESCRIPTION

The following paragraphs describe the functional description for the 10 and 20 megabyte disk drives. This information provides maintenance personnel with a comprehensive understanding of the functions of the drive. A brief discussion of disk recording principles is followed by a functional description of the disk drive unit, explaining how the drive interfaces with the controller and describes interface signals. The physical locations of the logics and their interconnections are shown in the detailed diagram of figure 7-8.

7.3.1 Basic Disk Principles

The recording medium for the drive is a stack of two or four 5 1/4-inch disks with four to eight recording surfaces (see figure 7-9).

Each disk is coated with a layer of magnetic oxide. The coating is burnished to a flatness that allows the read/write heads to fly in proximity to the surface without actual physical contact.

Data is recorded in serial fashion on concentric rings on each disk surface by holding the head in a fixed position over the rotating disk. These rings are referred to as tracks. The disk drive unit positions the heads precisely over the tracks. Corresponding track positions, both upper and lower on each disk, are referred to as one cylinder of data.

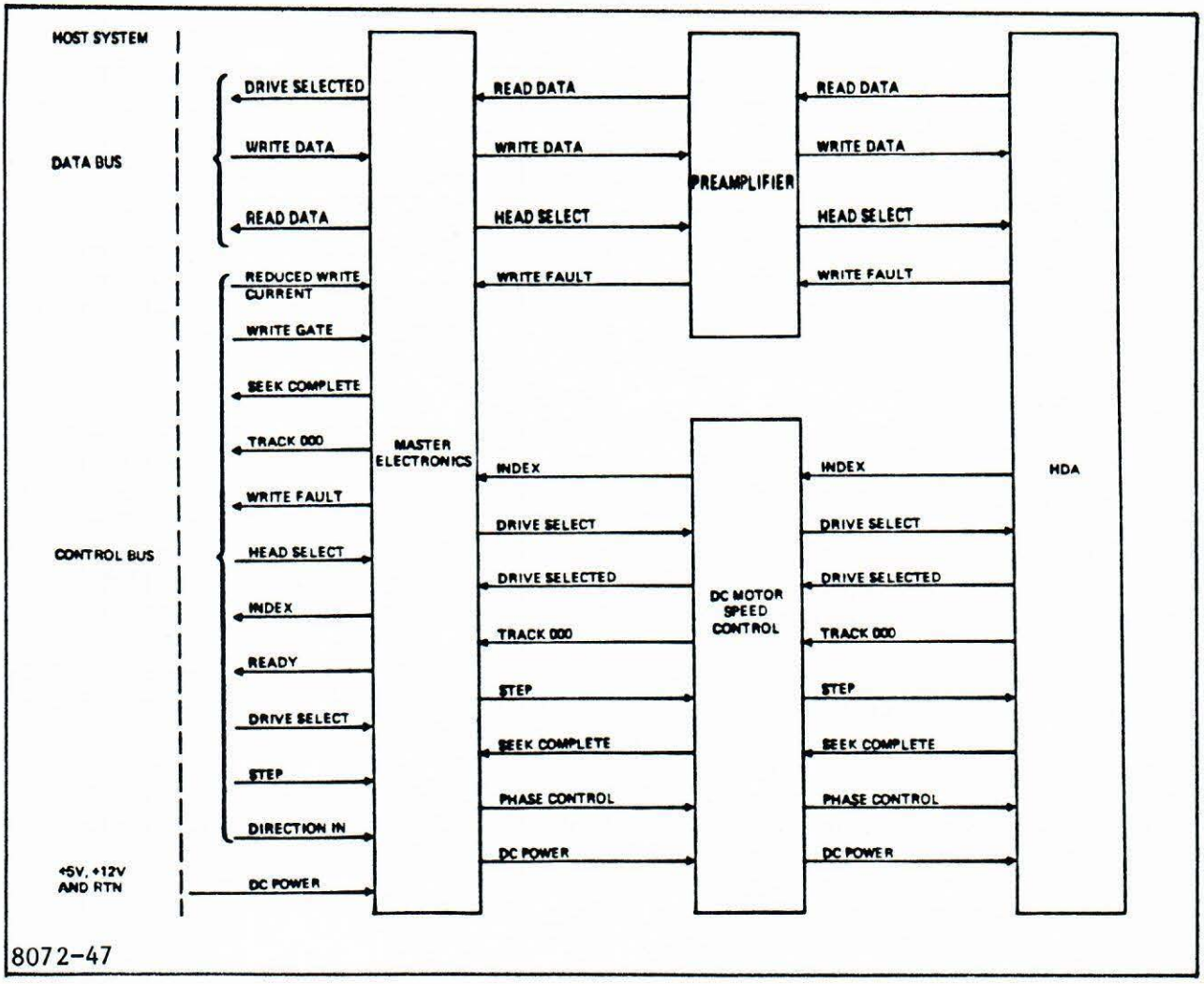

Figure 7-8. Disk Drive Block Diagram

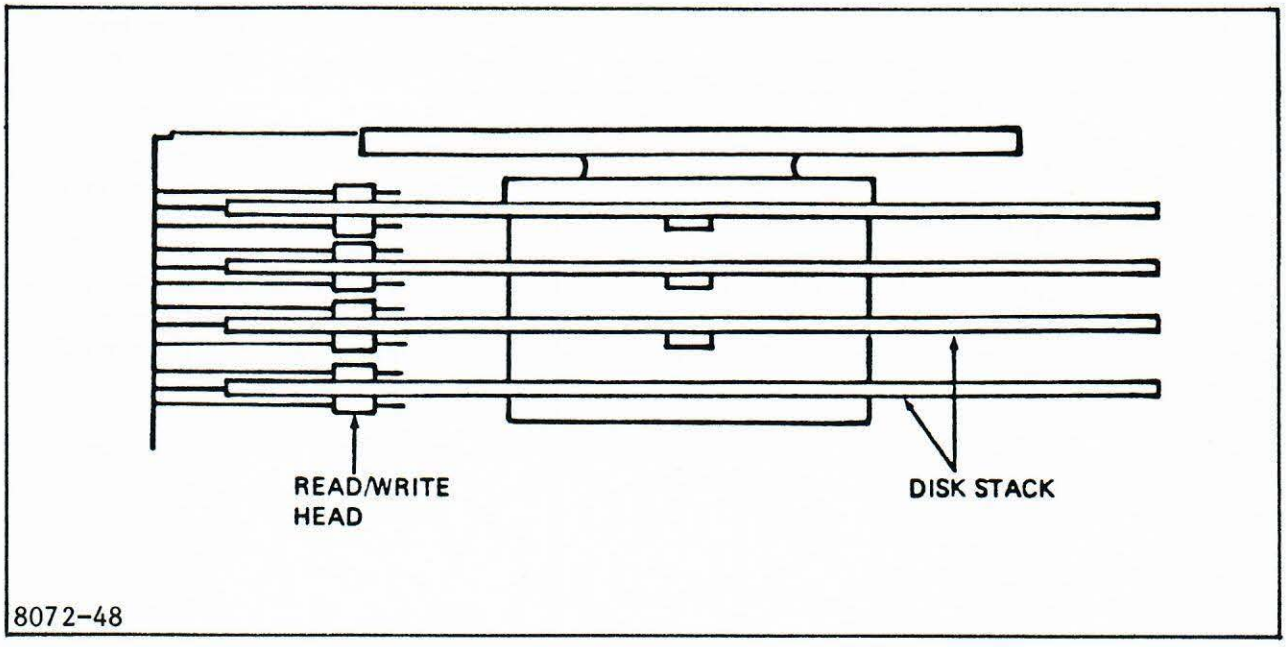

Figure 7-9. Surface and Head Geometry

A center-tapped coil is mounted on the core of the read/write head to perform the read/write function. The recording flux direction is controlled by energizing the center-tap connection, causing current to flow through the bifiler winding from the center tap to either one end or the other. When reading, the ends of the coil are switched to the input of the read amplifier. Data is erased by writing new data on the track. The read/write coil is mounted onto the core of the ferrite slider. As the disk rotates, it pulls a film of air around its surface. This moving air moves under the slider and exerts an upward force on the shoe. A downward pressure is placed on the slider by the spring flexure of the head. The head shoe then flies at a point where the downward force of the load spring is equal in force to the air pressure under the head.

The flying height of the slider is influenced in part by the air-bleed channel in the middle of the slider. This channel allows some air to bleed from under the slider, decreasing the air pressure and allowing the head to fly closer to the disk surface. The average flying height of the head is 19 microinches. (The head is closer on an inner track because the inner track portion of the disk is moving at a slower speed than the outer track portion of the disk, resulting in less air pressure on the inner track than on the outer track.)

The slider is mounted to the head arm assembly via a spring gimbal-mount. This allows the flying attitude of the slider to vary slightly so that it can follow minor surface variations without contacting the disk surface.

All heads are mounted on a carriage so that the heads and carriage move as one unit. The carriage moves the heads radially over the disk's surfaces. All the heads are positioned to the same cylinder at any given time.

7.3.2 Control Lines

The control data is exchanged between drive and control unit via the control cable. The following paragraphs define the control interface signals.

Reduced Write Current - The Reduced Write Current signal from the host system enables a current sink during a write, diverting current from the head and effectively reducing the write current.

Write Gate - When True, the Write Gate signal from the host enables the current source and Write drive signals. When False, this signal enables Read Data to be transferred from the drive to the host.

Seek Complete - The Seek Complete status signal is generated by the microprocessor in the master electronics board when the value of an internal 8-bit counter equals the desired stepper motor phase changes (determined by the Step and Direction In input signals).

Track 000 - The Track 000 status line is set true when the read/write heads are positioned over track 00.

Write Fault - The Write Fault signal is true under the following fault conditions:

a. Write current in a head when Write Gate is false.

b. No write current in any head when both Write Gate and Drive Selected are true.

c. More than one head is selected.

d. The 12-volt supply is below 10.3 volts.

e. The 5-volt supply is below 4.5 volts.

f. Motor speed exceeds ±1% tolerance at the end of the power-up sequence.

g. Motor speed exceeds ±10% tolerance.

h. No Index signal.

i. Motor not up to speed.

j. Step signal received while Write Gate is true.

Head Select - Up to eight read/write heads may be selected using a 3-bit code on the Head Select 0, Head Select 1 and Head Select 2 lines. Table 7-5 is a head select matrix showing the logic level required on each Head Select line to select the desired read/write head.

Table 7-5. Head Select Decode Matrix

LINE	HD0	HD1	HD2	HD3	HD4	HD5	HD6	HD7
Head Select 0	False	True	False	True	False	True	False	True
Head Select 1	False	False	True	True	False	False	True	True
Head Select 2	False	False	False	False	True	True	True	True

Index - The Index signal is a 200 microsecond output pulse used to mark a fixed reference point relative to the disk.

Ready - The Ready signal is true when the drive is ready to read or write (with or without am implied seek) and the other lines are valid. Ready remains true until power-off or until there is a Write Fault. The Ready signal is false under the following conditions:

a. The drive is undergoing power-up.

b. Motor speed is out of tolerance (+10%, -5% of nominal).

c. Write Fault is true.

Drive Select - The Drive Select signal from the host system corresponds with the drive select switch setting of the drive. If the Drive Select signal does not correspond, and the Ready signal is true, a Drive Selected true signal is returned to the host system via the data lines.

Step - The Step signal pulse from the host system is used in conjunction with the Direction In signal to move the stepper motor. This pulse input to the microprocessor is used to clock an internal 8-bit counter which is reset prior to each seek. Once the first step pulse is received, the processor issues stepper motor phase changes until the number of changes equals the value in the counter.

Direction In - The Direction In signal from the host controller determines the direction of motion of the stepper motor. The microprocessor receives the first step pulse of any seek, samples the input and internally stores the result.

7.3.3. Data Lines

The disk drive transmits and receives differential data coded in modified-frequency-modulation (MFM) via the data cable. Decoding is done by the host system. Precompensation (early and late) of write data is used for certain data patterns. The following paragraphs describe the read/write data, as well as the Drive Selected signal.

MFM Read Data - Data signals from the disk drive, recovered by reading a prerecorded track, are transmitted to the host system using an EIA RS-422 standard differential line driver, as shown in figure 7-10. This balanced voltage signal will drive up to 20 feet of twisted-pair or flat-ribbon cable with an impedance (Z) of 105 ohms. The recommended receiver is shown in figure 7-11. The transition of +MFM read data going more positive than -MFM read data represents a magnetic flux transition on the disk under the selected head. Timings are shown in figure 7-12.

MFM Write Data - The MFM write data is transmitted by the host system to the disk drive using a standard differential line driver. (The line driver and the line receiver are the same type as used in transmission of the read data. See figures 7-10 and 7-11.) The transition of the +MFM Write data going more positive than -MFM Write data results in a flux reversal on the disk under the selected head, provided Write Gate is true and the drive is selected (Drive Select is true). MFM write data is inactive when Write Gate is false.

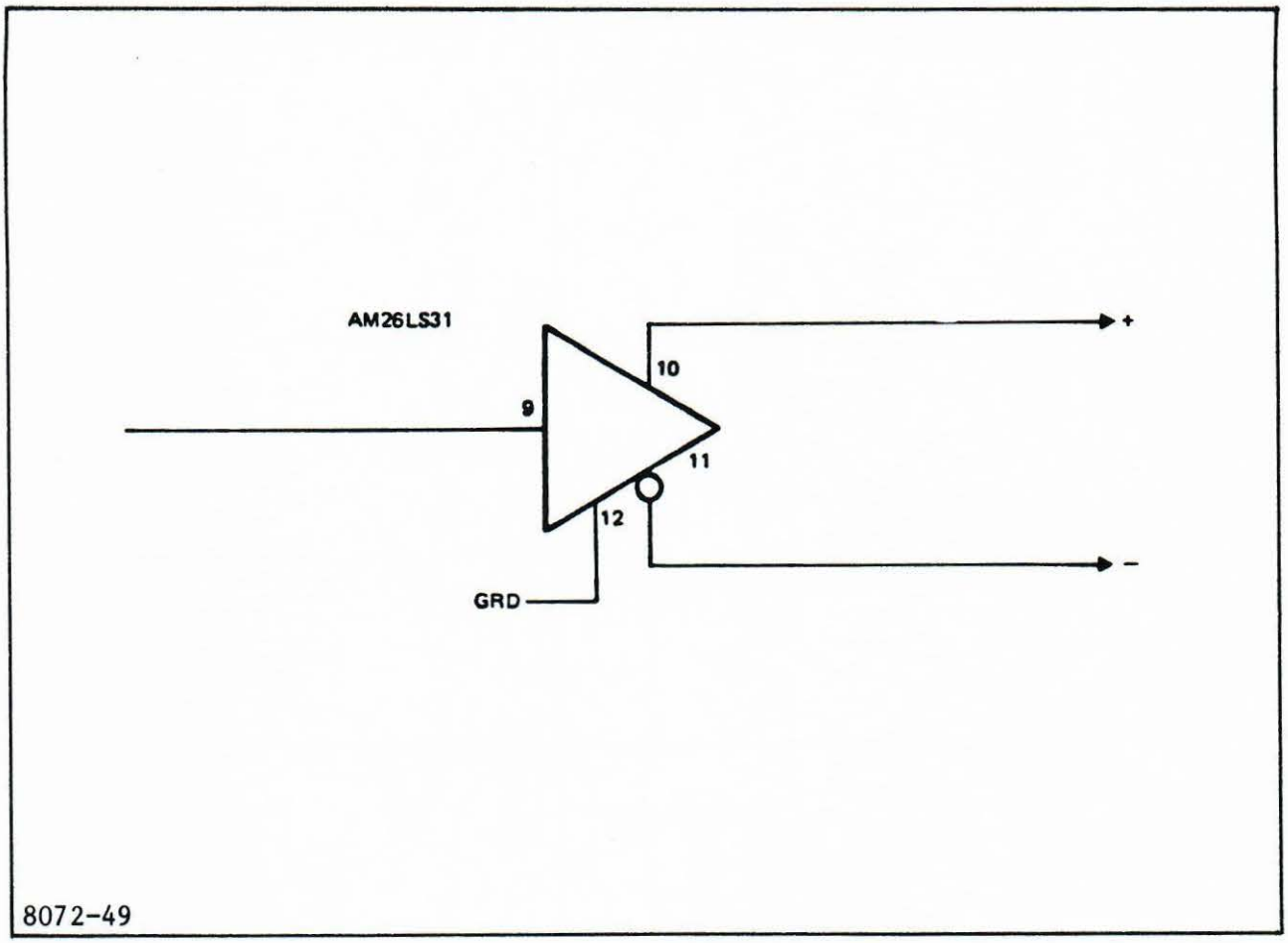

Figure 7-10. Differential Read Data Line Driver

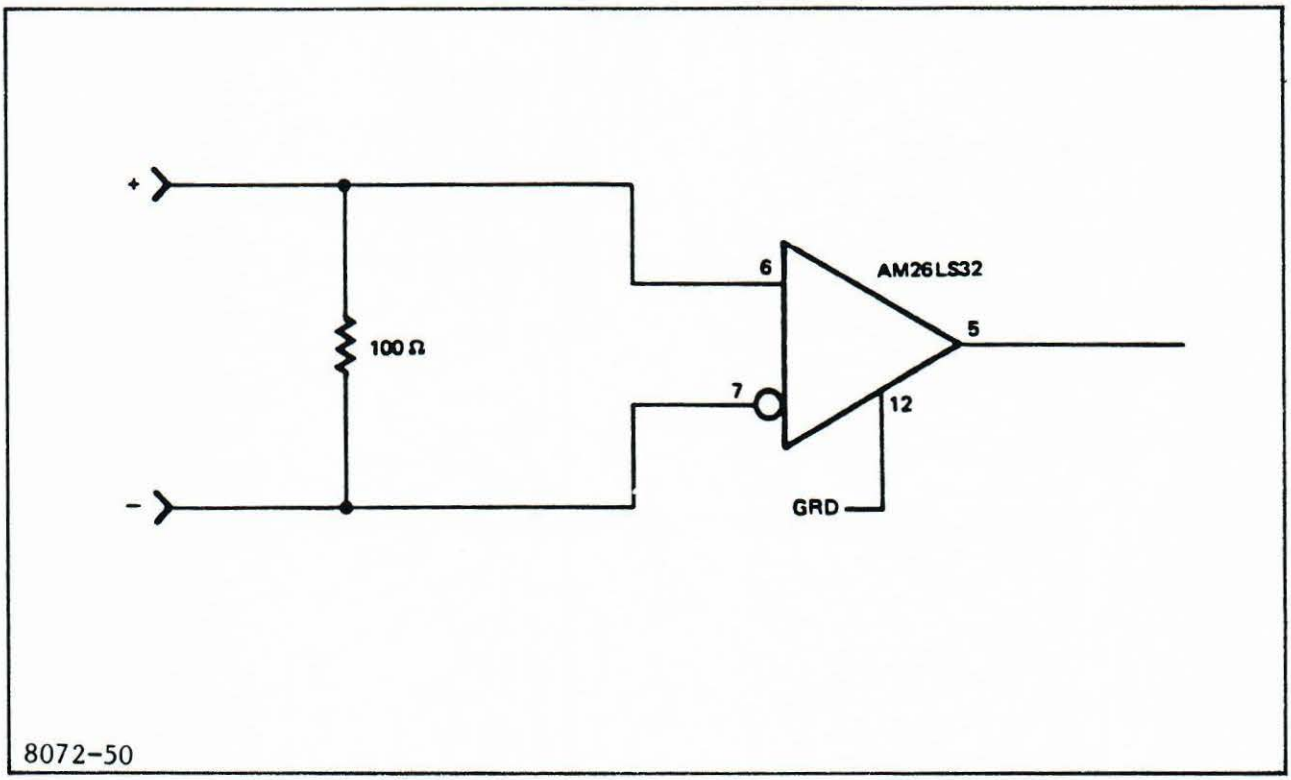

Figure 7-11. Differential Write Data Line Receiver

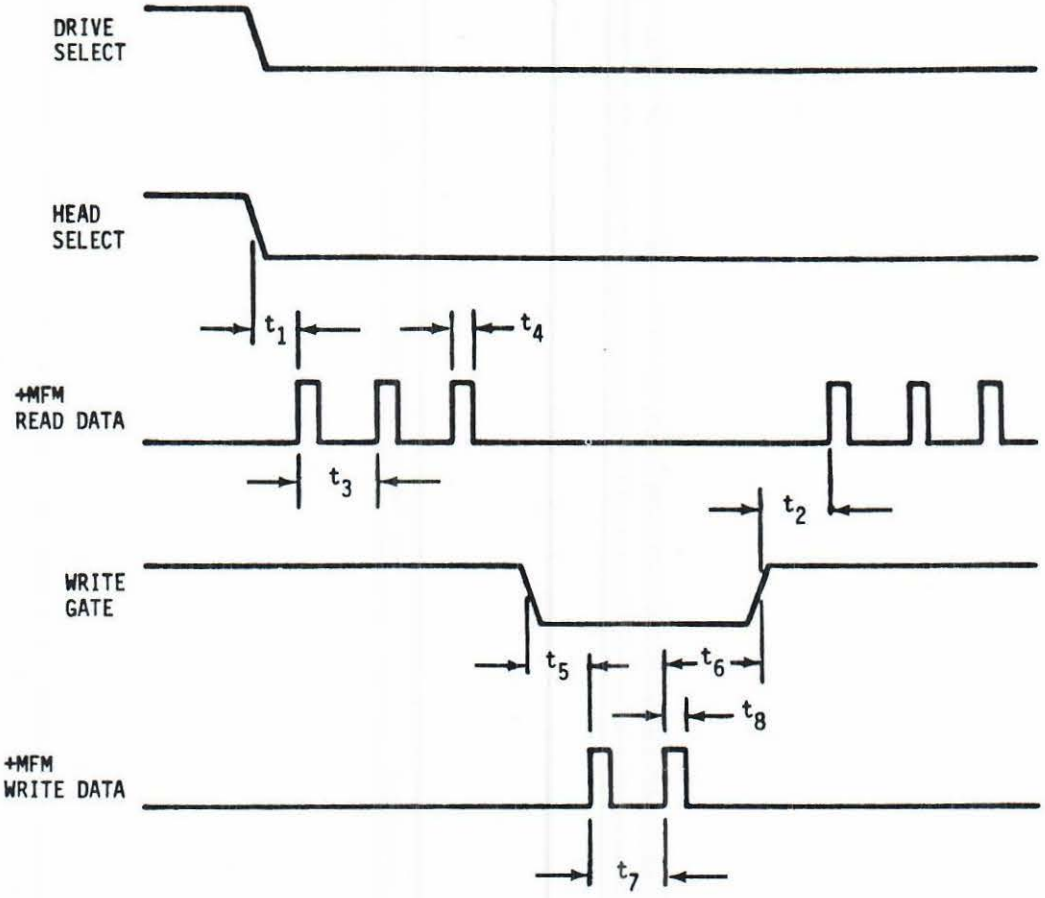

Figure 7-12. Read/Write Timing

Write Precompensation - During Write, it may be desirable to apply an advance or delay on MFM bits when they occur in certain patterns. This advance or delay compensates for peak shift on the disk due to pulse crowding. From an anyalysis of 4-bit sequences, a preferred precompensation scheme is shown in table 7-6 and figure 7-13. Late or early compensation applies only to the third bit of each pattern. No other patterns should be compensated.

The value of compensation should be 10 to 12 nanoseconds, and it is recommended that the value apply to all cylinders.

Table 7-6. Write Data Precompensation

DATA SEQUENCE	DIRECTION OF SHIFT
DCBA	
0000	On Time Clock
0001	Late Clock
0010	On Time Data
0011	Early Data
0100	--
0101	--
0110	Late Data
0111	On Time Data
1000	Early Clock
1001	On Time Clock
1010	On Time Data
1011	Early Data
1100	--
1101	--
1110	Late Data
1111	On Time Data

7.3.4 Disk Controller

The controller is contained on a single printed circuit board. Because the controller uses the Shugart Associates System Interface (SASI), it does not require special or complex design considerations in order to communicate with the host buses. The simplified block diagram in figure 7-14 shows functional organization of the controller. Only the major areas are shown, and are defined as follows:

- Host Interface - The host interface connects the internal data bus to the host adapter. The state machine controls the movement of data and commands through the host interface.
- Processor - The eight-bit processor is the intelligence of the controller; it monitors and controls the operation of the controller.
- State Machine - The state machine controls and synchronizes the operation of the host adapter, SERDES, and sector buffer.

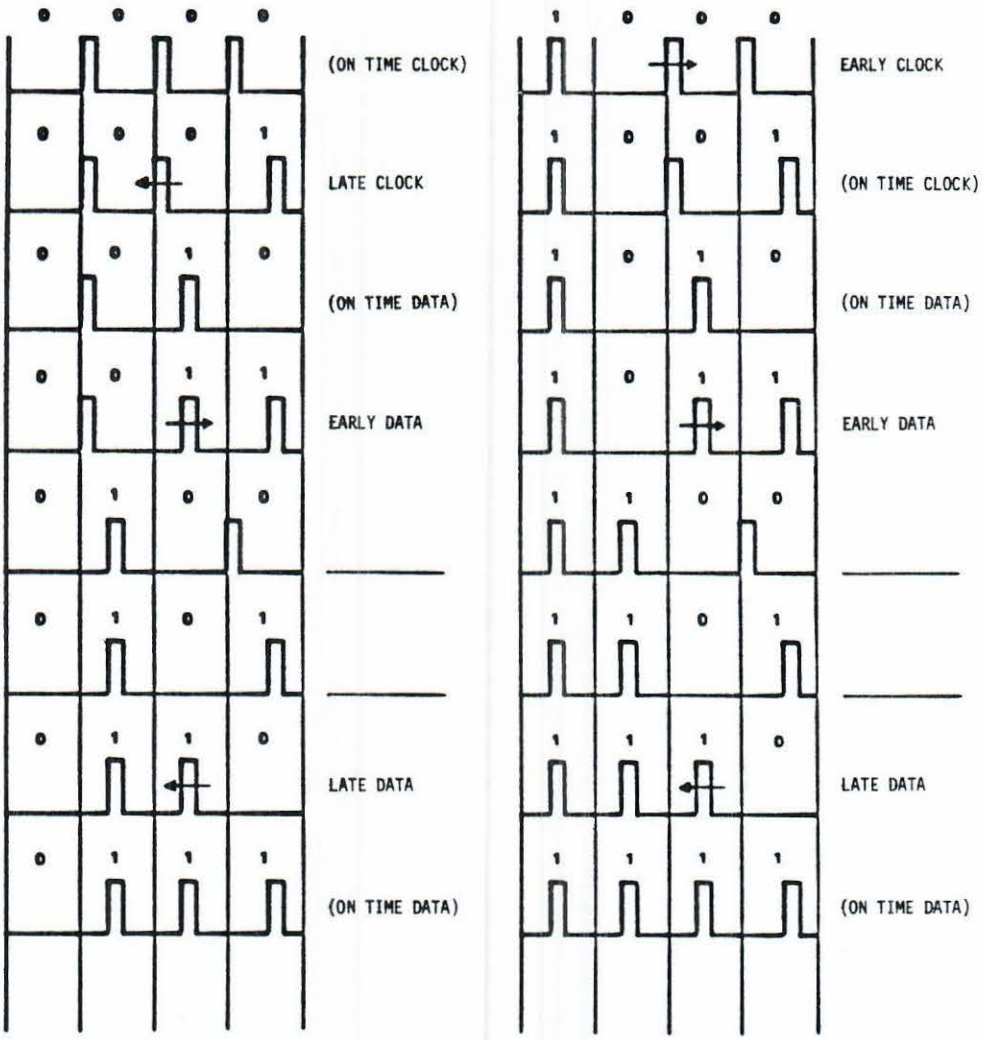

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Figure 7-13. Write Data Precompensation

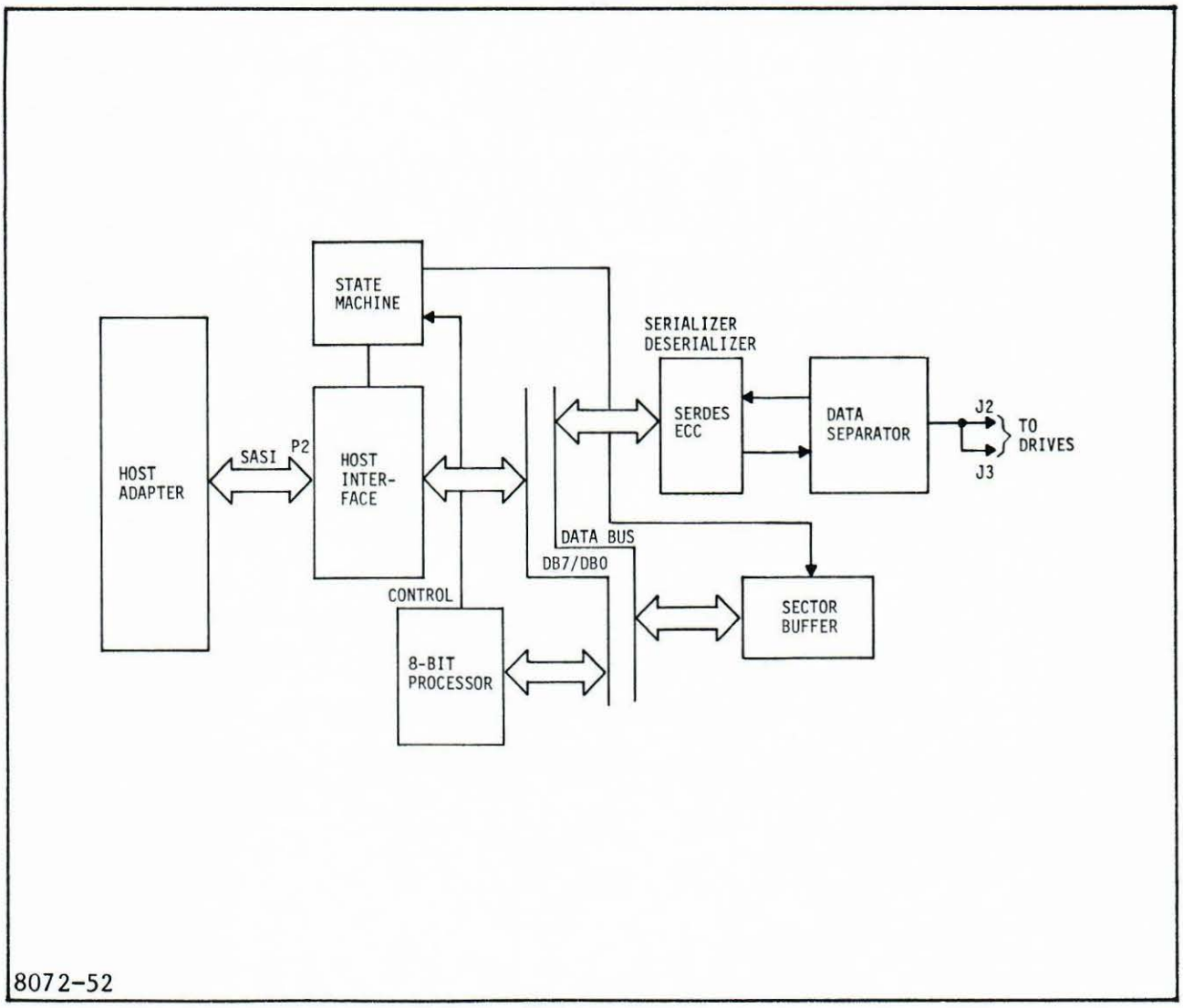

Figure 7-14. Controller, Functional Organization

- SERDES - The serializer/deserializer (SERDES) converts parallel data from the internal data bus to serial data for transfer to a selected disk drive. It converts serial data from the selected disk drive to parallel data which it places on the internal data bus.

- Data Separator - The data separator converts serial NRZ data to MFM for transfer to the selected disk drive. It converts MFM data coming from the selected disk drive to serial NRZ data for the SERDES.

- Sector Buffer - The sector buffer stages data transfers between the disk and the host to prevent data overruns.

7.3.4.1 Signal Definitions

Tables 7-7 thru 7-11 list and define the signals that appear on the SASI Bus lines between the host adapter and the controller.

The dash(-), or the lack of one, indicates the active state of a signal. The active state of a signal is that state which is required for a given operation. When a dash is appended to the end of a signal name, the signal is active when it is low. When no dash appears at the end of a signal name, the signal is active when it is high. Some signal lines have two so-called active (or significant) states. When the level on the line is high, a particular operation takes place. When the level on the line is low, a different operation takes place. The following examples show the use of these conventions.

- BUSY- The signal BUSY- is active when it is at low level because it has the dash appended.
- BUSY The signal BUSY is active at a high level because it does not have the dash appended.
- C-/D The line C-/D (command-/data) has a dual purpose; the slash (/) indicates quality. The dash after the C indicates that when this line is at a low level, command mode is indicated and when it is at a high level, data mode is indicated.

Other designations used to define signal lines are listed below.

- Drv Driver
- Rcvr Receiver
- OC Open collector
- Tri-State Line has three states: high, low, high impedance
- 220/330 Line termination: 220 Ohms to source voltage/330 Ohms to ground

Table 7-7. Host Bus Status Signals

NAME	DRV/RCVR	DEFINITION
I-/O	Drv OC	Input-/Output-: The controller drives this line. A low level on this line indicates that the controller is driving the data in on the host bus. A high level on this line indicates that the host adapter is driving the data out on the host bus. The host adapter monitors this line and uses it to enable and disable its data bus drivers. This signal is qualified by signal REQ-.
C-/D	Drv OC	Command-/Data: This signal line indicates whether the information on the data bus consists of command or data bytes. A low means command bytes; a high means data bytes. This signal is qualified by signal REQ-.

Table 7-7. Host Bus Status Signals (continued)

NAME	DRV/RCVR	DEFINITION
BUSY-	Drv OC	Busy: The controller generates this active low signal in response to the SEL- signal and the address bit (DB0- to DB7-) from the host adapter. The busy signal informs the host adapter that the controller is ready to conduct transactions on the host bus.
MSG-	Drv OC	Message: The controller sends this active low signal to the host adapter to indicate that the current command has been completed. When MSG- is active, the I-/O signal line is always low so that the controller can driver the bus data lines. This signal is qualified by signal REQ-.

Table 7-8. Summary of Host Bus Status Signals

I-/O	C-/D	MSG-	DEFINITION
High	Low	High	The controller receives command from the host adapter.
High	High	High	The controller receives data from the host adapter.
Low	High	High	The controller sends data to the host adapter.
Low	Low	High	The controller sends error status byte to the host adapter.
Low	Low	Low	The controller informs the host adpater that it has completed the current command.

Table 7-9. Controller - Host Handshaking

NAME	DRV/RCVR	DEFINITION
REQ-	Drv OC	Request: The controller sends this active low signal to the host adapter for each byte transferred across the interface. This signal qualifies signals I-/O, C-/D and MSG-.
ACK-	Rcvr, 220/330	Acknowledge: The host adapter generates this active low signal in response to the REQ- signal from the controller when the host is ready to receive or transmit a byte of data. In order to complete the handshake, the host adapter must send an acknowledge (ACK-) in response to each request (REQ-) from the controller.

Table 7-10. Host Bus Control Signals

NAME	DRV/RCVR	DEFINITION
RST-	Rcvr, 220/220	Reset: The host adapter sends this active low signal to the controller to force the controller to the idle state. After RST- has become active, any controller status is cleared. RST- also causes the deactivation of all signals to the drives. The time requirement for the RST- signal is as follows: Minimum: 100 nsec. Maximum: None
SEL-	Rcvr, 220/330	Select: The host adapter sends this active low signal to the controller to initiate a command transaction. Along with SEL-, the host adapter must also send an address bit to select the controller (DBO- for controller). The controller must not be busy. The host adapter must deactivate SEL- before the end of the current command.

Table 7-11. Host Bus Data Signals

NAME	DRV/RCVR	DEFINITION
DB7- to DBO-	Tri-State 220/330	These are the eight data bits (lines) of the host bus (DBO = LSB). Each line is also used as address bits to select a controller in systems using multiple controllers. The normal connnection (hardwired on the board) is to DBO- which is the address of controller 0. Any other connection requires cutting the existing trace on the board and adding a jumper. The following list shows the bit assignments. DBO- Controller 0 DB1- Controller 1 DB2- Controller 2 DB3- Controller 3 DB4- Controller 4 DB5- Controller 5 DB6- Controller 6 DB7- Controller 7

7.3.4.2 Detailed Description (Handshaking and Timing)

The following paragraphs describe the interaction between the controller and the host adapter.

Controller Selection - Before the host adapter can begin a transaction, it must select the controller. The host adapter selects the controller by activating the SEL- control signal and the address bit of the controller. Any bit, DB0- through DB7-, can be the address bit in a system with multiple controllers (all controllers leave the factory with DB0- connected to the controller's address logic). For this discussion, the controller's address is 0.

The timing diagram in figure 7-15 shows the basic timing requirements. Upon receiving both the SEL- signal and DB0-, the controller activates the BUSY- signal. As shown in the timing diagram, both SEL- and DB0- must be active (low) before the controller can activate the BUSY- signal. During the selection process, the host has control of the data bus as signified by the deactivation of the I-/O line. Selection is complete when BUSY- becomes active. The SEL- signal must be deactivated by the host interface before the current controller operation has completed. It is recommended that the SEL- line be deactivated at or before the time the first command byte is sent to the controller. The controller then enters the command mode.

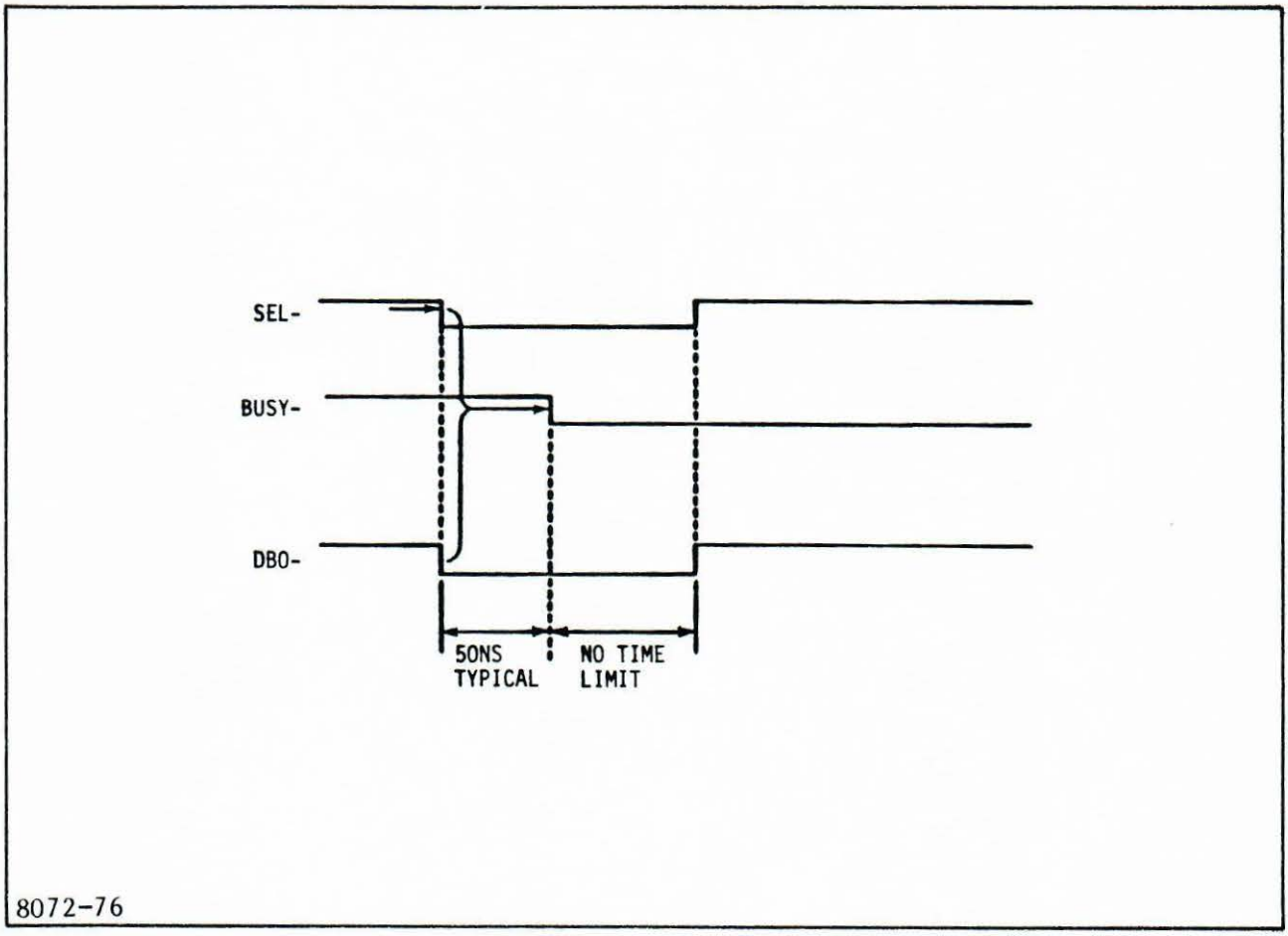

Figure 7-15. Controller Select Timing

Command Mode - The controller receives commands from the host adapter using a handshaking sequence. The controller places a low level on the C-/D (command-/data) line to indicate that it wants a command from the host adapter and places a high level on the I-/O line to indicate that the movement of information is from the host adapter out to the controller. The MSG- line is high.

The controller activates the REQ- line within 10 microseconds after signals I-/O, C-/D and MSG- have been placed at high, low and high levels, respectively. The host adapter responds by activating the ACK- signal when a command byte is ready for the controller. The command byte placed on the data bus by the host must be stable within 250 nanoseconds after the ACK- signal is activated. The command byte must be held stable until REQ- is deactivated. The host deactivates ACK- after REQ- goes high. This completes the handshake for the first command byte. Each succeeding command byte from the host adapter requires the same complete handshake sequence. See figure 7-17 for for data bus, REQ-, and ACK- timing. See table 7-7 for I-/O, C-/D and MSG- definition.

Data Transfer - The timing diagrams in figures 7-16 and 7-17 illustrate the required timing for data transfer. See table 7-7 for I-/O, C-/D and MSG- definition.

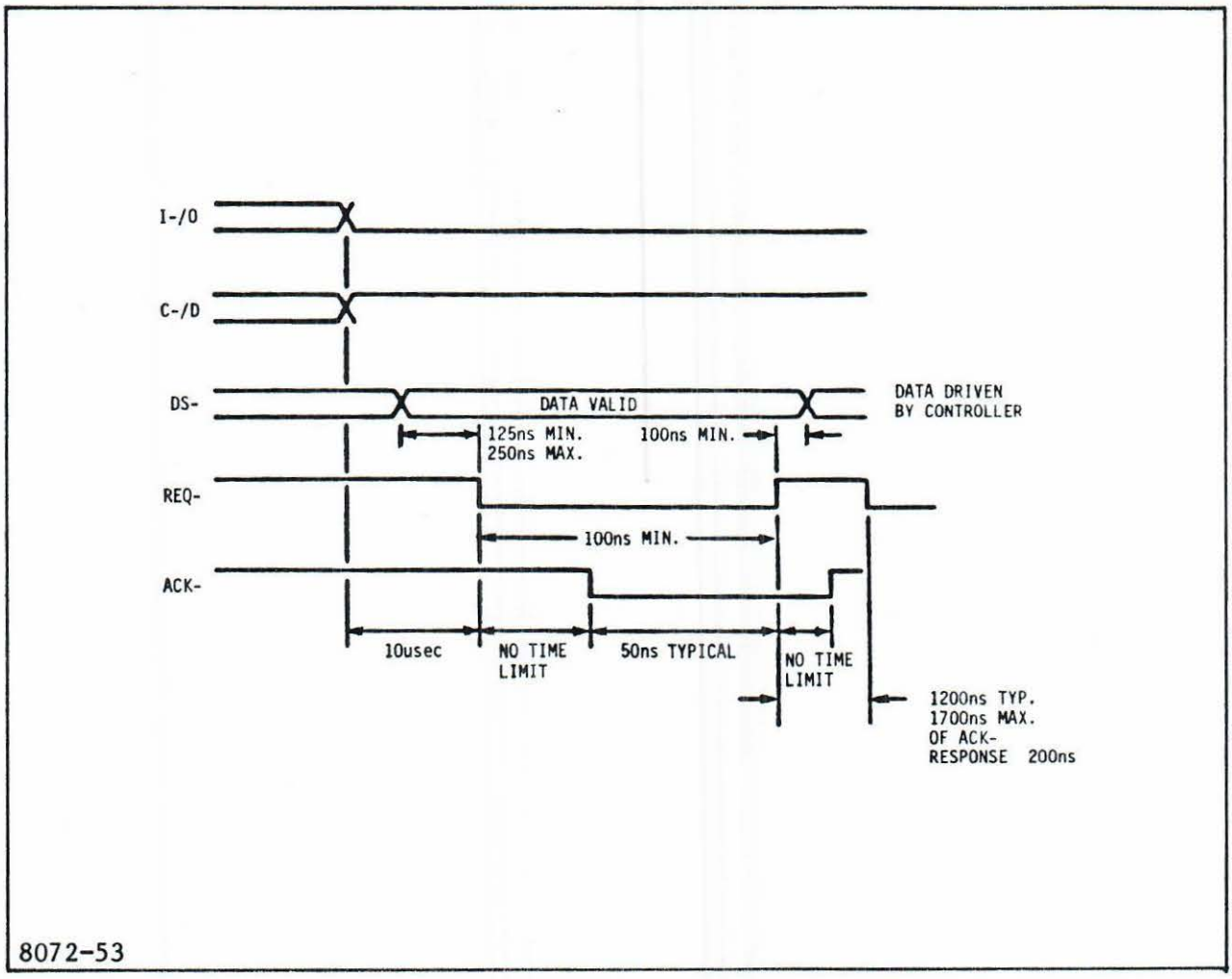

Figure 7-16. Data Transfer to Host, Timing

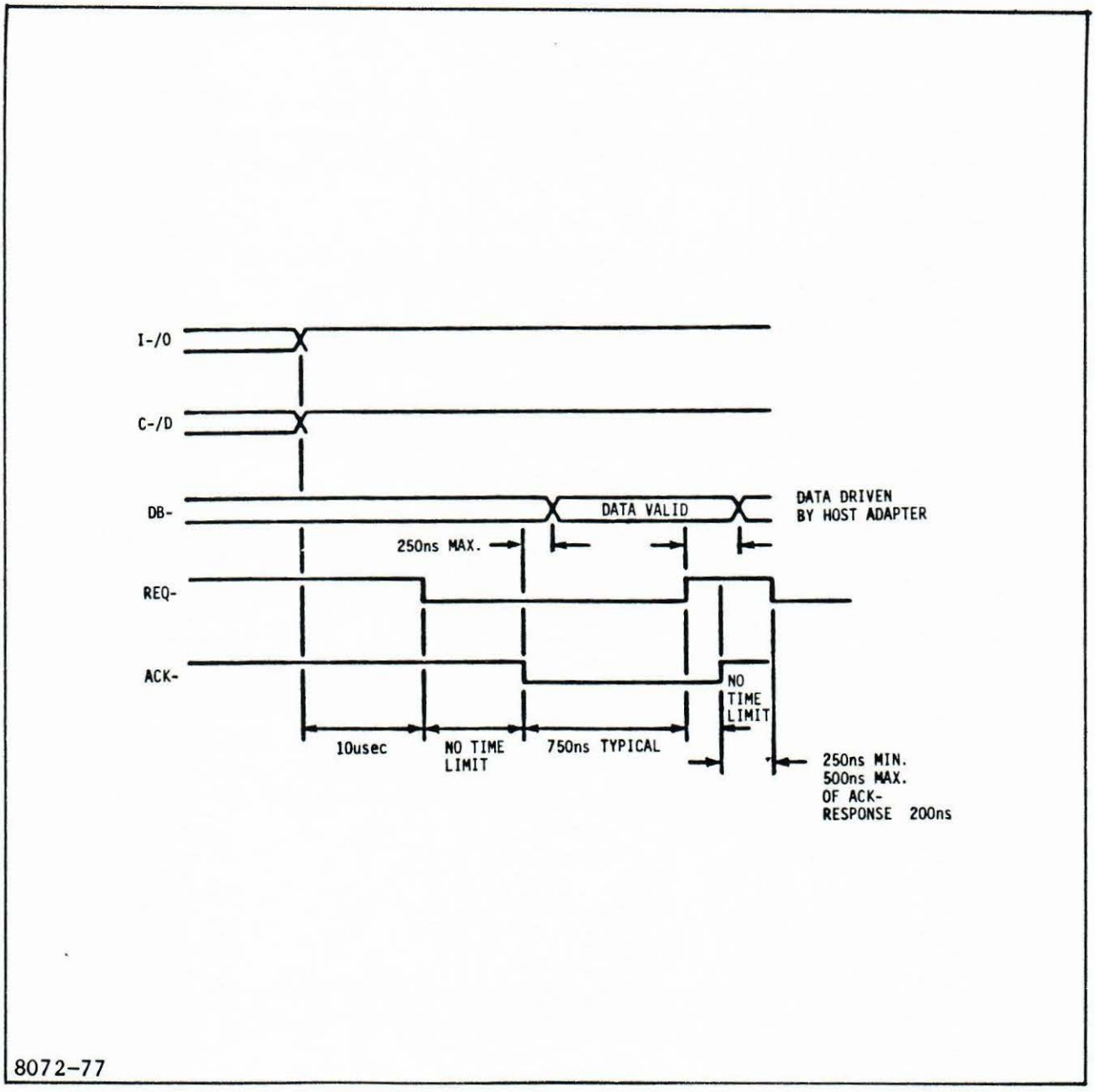

Figure 7-17. Data Transfer from Host, Timing

Status Bytes - Two bytes of status are passed to the host at the end of all commands. The first byte informs the host if any errors occurred during the execution of the command. The second is a zero byte. It signals to the host that the command is complete. Figure 7-16 shows the data bus, REQ- and ACK- timing. See table 7-7 for I-/O, C-/D and MSG- definition. Figure 7-19 shows the format of these two bytes.

7.3.4.3 Programming Information

The following section discusses communications between the controller and host from the point of view of the codes that are passed. The host sends commands to the controller through the host adapter. The controller then performs the commands and reports back to the host.

7.3.4.4 Commands

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). Figure 7-18 shows the composition of the DCB. The list that follows figure 7-18 defines the bytes that make up the DCB.

At the end of a command, the controller returns two completion status bytes to the host. The format of these bytes is shown in figure 7-19.

Control Byte - The control field, byte 5, of the DCB allows the user to select options for several different types and makes of disk drives. The following list defines the bits of the control byte.

Bit 0 Half-step option of Seagate and Texas instrument drives.

Bit 1 Half-step option for Tandon drives.

Bit 2 Buffer-step option for drives made by Computer Memories, Inc. and Rotating Memories, Inc. (200 microsecond pulse per step).

Bit 3-5 Spare. Set to zero for future use.

Bit 6 If one, during a read sector command, the failing sector is not re-read on the next revolution before attempting correction. This bit should be set to zero for normal operation.

Bit 7 Disable the retries by the controller on all disk-access commands. Set this bit only during the evaluation of the performance of a disk drive. This bit should be set to zero for normal operation.

NOTE

The step option bits (2-0) are mutually exclusive and only one option should be selected in any given configuration.

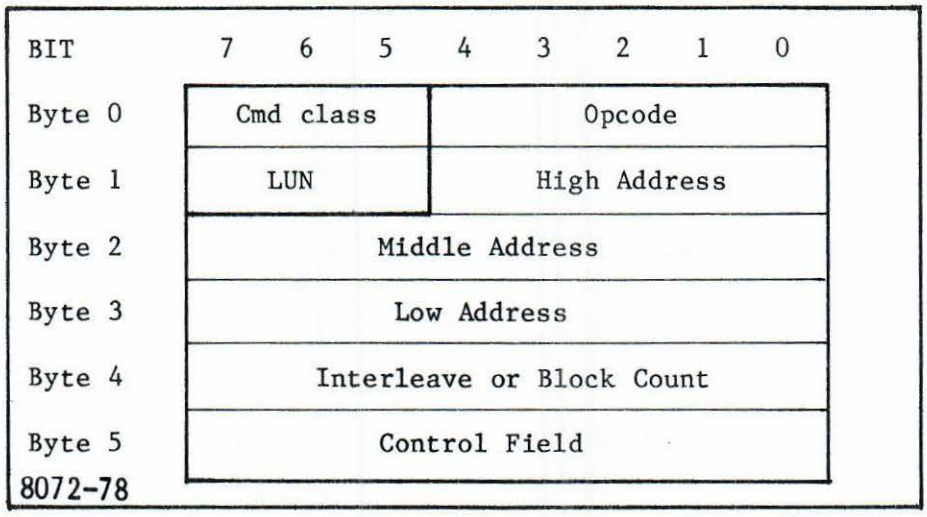

Figure 7-18. Device Control Block (DCB) Format

Byte 0	Bits 7, 6 and 5 identify the class of the command Bits 4 through 0 contain the opcode of the command
Byte 1	Bits 7, 6 and 5 identify the logical unit number (LUN) Bits 4 through 0 contain logical disk address 2
Byte 2	Bits 7 through 0 contain logical disk address 1
Byte 3	Bits 7 through 0 contain logical disk address 0 (LSB)
Byte 4	Bits 7 through 0 specify the interleave or block count
Byte 5	Bits 7 through 0 contain the control field.

Next to Last Status Byte

BIT	7	6	5	4	3	2	1	0
	0	0	d	0	0	0	ERR	0

Bits 0, 2-4,6,7	Set to zero
Bit 1	When set, error occurred during command execution
Bit 5	Logical unit number of drive, d=0 or 1

Last Status Byte

BIT	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

Bits 0-7	Set to zero

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Figure 7-19. Completion Status Bytes

Logical Address (High, Middle and Low) - The logical address of the drive is computed by using the following equation.

Logical Address = (CYADR o HDCYL + HDADR) o SETRK + SEADR

Where: CYADR = Cylinder Address
HDARD = Head Address
SEADR = Sector Address
HDCYL = Number of Heads per Cylinder
SETRK = Number of Sectors per Track

The commands fall into eight classes, 0 through 7; only classes 0 and 7 are used. Class 0 commands are data, non-data transfer, and status commands. Classes 1 through 6 are reserved. Class 7 are diagnostic commands.

Each command is described on the following page. The description includes its class, opcode, and format. When a slash (/) represents a bit position, the slash means that the value of that bit is not important (a don't-care bit).

Test Drive Ready (Class 0, Opcode 00) - This command selects a particular drive and verifies that the drive is ready. The following diagram shows the format of the device control block for this command.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

Recalibrate (Class 0, Opcode 01) - This command positions the read/write (R/W) arm to track 00.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	r	/	/	/	/	s	s	s

Reserved (Class 0, Opcode 20) - This opcode is not used.

Request Sense Status (Class 0, Opcode 03) - The host must send this command immediately after it detects an error. The command causes the Controller to return four bytes of drive and Controller status: the formats of these four bytes are shown after the DCB. When an error occurs on a multiple sector data transfer, (read or write), the Request Sense Status command returns the logical address of the failing sector in bytes 1, 2 and 3. If the Request Sense Status command is issued after any of the Format commands or the Check Track Format command, then the logical address returned by the controller points to one sector beyond the last track formatted or checked if there was no error. If there was an error, then the logical address returned points to the track in error. Tables 7-12 through 7-15 that follows the formats list the error codes.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

SENSE BYTES

BIT	7	6	5	4	3	2	1	0
Byte 0	SEE BELOW							

Bits 0-3 Error Code
Bits 4-5 Error Type
Bit 6 Spare, set to zero
Bit 7 Address valid, when set

The address valid bit in the error code byte (bit 7) is relevant only when the previous command required a logical block address; in which case it is always returned as a one otherwise it is set to zero. For instance, if a Recalibrate command is followed immediately by a Request Sense Status command, the address valid bit would be returned as zero since this command does not require a logical block address to be passed in its DCB.

d = drive, 0 or 1

BIT	7	6	5	4	3	2	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							

Table 7-12. Type 0 Error Codes, Disk Drive

HEX CODE	DEFINITION
0	The controller detected no error during the execution of the previous operation
1	The controller did not detect an index signal from the drive
2	The controller did not get a seek complete signal from the drive after seek operation
3	The controller detected a write fault from drive during last operation
4	After the controller selected the drive, the drive did not respond with ready signal
5	Not used
6	After stepping maximum number of cylinders, controller did not receive track 00 signal from the drive

Table 7-13. Type 1 Error Codes, Controller

HEX CODE	DEFINITION
0	ID Read Error: The controller detected an ECC error in the target ID field on the disk
1	Data Error: The controller detected an uncorrectable ECC error in the target sector during a read operation
2	Address Mark: The controller did not detect the target address mark (AM) on the disk
3	Not used
4	Sector Not Found: The controller found the correct cylinder and head, but not the target sector
5	Seek Error: The controller detected an incorrect cylinder or track, or both
6	Not used
7	Not used
8	Correctable Data Error: The controller detected a correctable ECC error in the target data field
9	Bad Track: The controller detected the bad track flag during the last operation
A	Format Error: During a check-track command, the controller detected one of the following: • track not formatted • wrong interleave • ID ECC error on at least one (1) sector

Table 7-14. Types 2 and 3 Error Codes, Command and Miscellaneous

HEX CODE	TYPE	DEFINITION
0	2	Invalid Command: The controller has received an invalid command from the host
1	2	Illegal Disk Address: The controller detected an address that is beyond the maximum range
0	3	RAM Error: The controller detected a data error during the RAM sector buffer diagnostic
1	3	Program Memory Checksum Error: During its internal diagnostic, the controller detected a program-memory checksum error
2	3	ECC Polynominal Error: During the controller's internal diagnostic, the hardware ECC generator failed its test.

The following is a summary of the error codes returned as the result of the Request Sense Status command.

NOTE: The address valid bit (bit 7) may or may not be set and is not included here for clarity.

Table 7-15. Request Sense Status Error Codes

ERROR CODE (HEX)	DEFINITION
00	No error detected (command completed okay)
01	No index detected from disk drive
02	No seek complete from disk drive
03	Write fault from disk drive
04	Drive not ready after it was selected
05	Not used
06	Track 00 not found
07-0F	Not used
10	ID field read error
11	Uncorrectable data error
12	Address mark not found
13	Not used
14	Target sector not found
15	Seek error
16-17	Not used
18	Correctable data error
19	Bad track flag detected
1A	Format error
1B-1F	Not used
20	Invalid command
21	Illegal disk address
22-2F	Not used
30	Ram diagnostic failure
31	Program memory checksum error
32	ECC diagnostic failure
33-3F	Not used

Format Drive (Class 0, Opcode 04) - This command formats all sectors with ID and data fields according to the selected interleave factor. Also, it writes 6C Hex into data fields. The starting address is passed in the DCB. The Controller will format from the starting address to the end of the disk.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	0	s	s	s

Interleave: 1 to 31 for 256 sectors
1 to 16 for 512 sectors

Check Track Format (Class 0, Opcode 05) - This command checks the format on the specified track for correct ID and interleave. The command does not read the data field.

d = drive, 0 or 1

r = retires

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	0	s	s	s

Interleave: 1 to 31 for 256 sectors
1 to 16 for 512 sectors

Format Track (Class 0, Opcode 06) - This command formats a specified track and can be used to clear bad-sector flag in all sectors on the specified track that was previously formatted with the Format Bad Track command. The command writes 6C Hex into all data fields.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	0	s	s	s

Interleave: 1 to 31 for 256 sectors
1 to 16 for 512 sectors

Format Bad Track (Class 0, Opcode 07) - This command formats the specified track and sets the bad-sector flag in the ID fields. It does not write the data fields.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	0	s	s	s

Interleave: 1 to 31 for 256 sectors
1 to 16 for 512 sectors

Read (Class 0, Opcode 08) - This command reads the specified number of sectors, starting with the initial sector address contained in the DCB.

d = drive, 0 or 1

r = retries

a = retry option on data ECC error

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	a	0	0	0	s	s	s

Reserved (Class 0, Opcode 09) - This opcode is not used.

Write (Class 0, Opcode 0A) - This command writes the specified number of sectors, starting with the initial sector address contained in the DCB. Each sector of data can be either 256 or 512 bytes long. The sector size is jumper selectable.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	0	0	0	0	s	s	s

Seek (Class 0, Opcode 0B) - This command initiates a seek to the track specified in the DCB. The drive must be formatted.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	/	/	/	/	/	/	/	/
Byte 5	r	0	0	0	0	s	s	s

Initialize Drive Characteristics (Class 0, Opcode 0C) - This command enables the user to configure the Controller to work with drives that have different capacities and characteristics. However, both drive 0 and drive 1 must be of the same manufacturer and model number.

After the host sends the command (DCB) to the controller, it then sends an eight-byte block of data that contains the drive parameters. Some of the parameters occupy two bytes; all two-byte paramteres are transferred with the most significant byte (MSB) first. The eight bytes are listed below.

C = Maximum number of cylinders (2 bytes)
H = Maximum number of heads (1 byte)
W = Starting reduced write current cylinder (2 bytes)
P = Starting write precompensation cylinder (2 bytes)
E = Maximum ECC data burst length (1 byte)

When the controller is powered up or reset, the default values listed below are set.

Maximum number of cylinders = 153
Maximum number of heads = 4
Starting reduced write current cylinder = 128
Starting write precompensation cylinder = 64
Maximum ECC data burst length = 11 bits

The parameter for the maximum ECC burst length defines the length of a burst error in the data field that the controller will correct. The burst length is defined as the number of bits from first error bit to the last error bit. For example, the controller detected a 5-bit ECC error and the erroneous data appeared as C5 (1100 0101) before correction and could appear as D4 (1101 0100) after the correction. However, if the host has set the maximum ECC burst length at 4 bits, the controller would have to flag this data as uncorrectable. This is a type 1, code 1 error.

Command Bytes

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	0	0
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

Parameter Bytes

BIT	7	6	5	4	3	2	1	0
Byte 0	C	C	C	C	C	C	C	C
Byte 1	C	C	C	C	C	C	C	C
Byte 2	0	0	0	0	H	H	H	H
Byte 3	W	W	W	W	W	W	W	W
Byte 4	W	W	W	W	W	W	W	W
Byte 5	P	P	P	P	P	P	P	P
Byte 6	P	P	P	P	P	P	P	P
Byte 7	0	0	0	0	E	E	E	E

Read ECC Burst Error Length (Class 0, Opcode 0D) - This command transfers one byte to the host. This byte contains the value of the ECC burst length that the controller detected during the last Read command. This byte is valid only after a correctable ECC data error, type 1, code 8.

BIT	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	0	1
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

RAM Diagnostic (Class 7, Opcode 00) - This command performs a data pattern test on the RAM buffer.

BIT	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	0	0
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

Reserved (Class 7, Opcode 01) - This opcode is not used.

Reserved (Class 7, Opcode 02) - This opcode is not used.

Drive Diagnostic (Class 7, Opcode 03) - This command tests both the drive and the drive-to-controller interface. The controller sends recalibrate and seek commands to the selected drive and verifies sector 0 of all the tracks on the disk. The controller does not perform any write operations during this command; it is assumed that the disk has been previously formatted.

BIT	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	1	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	r	0	0	0	0	s	s	s

Controller Internal Diagnostics (Class 7, Opcode 04) - This command causes the controller to perform a self-test. The controller checks its internal processor, data buffers, ECC circuitry, and the checksum of the program memory. The controller does not access the disk drive.

BIT	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	0
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

Read Long (Class 7, Opcode 05) - This command transfers the target sector and four bytes of data ECC to the host. If an ECC error occurs during the read, the controller does not attempt to correct the data field. This command is useful in recovering data from a sector that contains an uncorrectable ECC error. It is also useful during diagnostic operations.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	0	0	0	0	s	s	s

Write Long (Class 7, Opcode 06) - This command transfers a sector of data and four appended ECC bytes to the disk drive. During this write operation, the host supplies the four ECC bytes instead of the usual hardware-generated ECC bytes. This command is useful only for diagnostic operations.

d = drive, 0 or 1

r = retries

s = step option

BIT	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	0	0	0	0	s	s	s

7.3.4.5 Sector Format

Figure 7-20 shows the format of the sector and the names of the fields of the information traveling over the Controller-drive interface. Table 7-16 lists the fields and a description of each field.

Table 7-16. Sector Field Description

FIELD	BYTES	FIELD DESCRIPTION
AM	4	Address Mark
GAP1	9	Zero Byte Gap
SYNC1	1	ID Sync Byte
GAP2	2	ID Zero Byte Gap
COM	1	ID Compare Byte
CYLH	1	Cylinder High (MSB)
CYLL	1	Cylinder Low (LSB)
HEAD	1	Head Number
SEC	1	Sector Number
FLAG	1	Flag Byte
ZER	1	Zero Byte
ECC1	4	ID ECC Bytes
GAP3	16	Zero Byte Gap
SYNC2	1	Data Field Sync Byte
GAP4	2	Data Field Zero Byte Gap
DATA	256/512	Data Field
ECC2	4	Data Field Ecc Bytes
GAP5	14/43	Inter-record Zero Gap

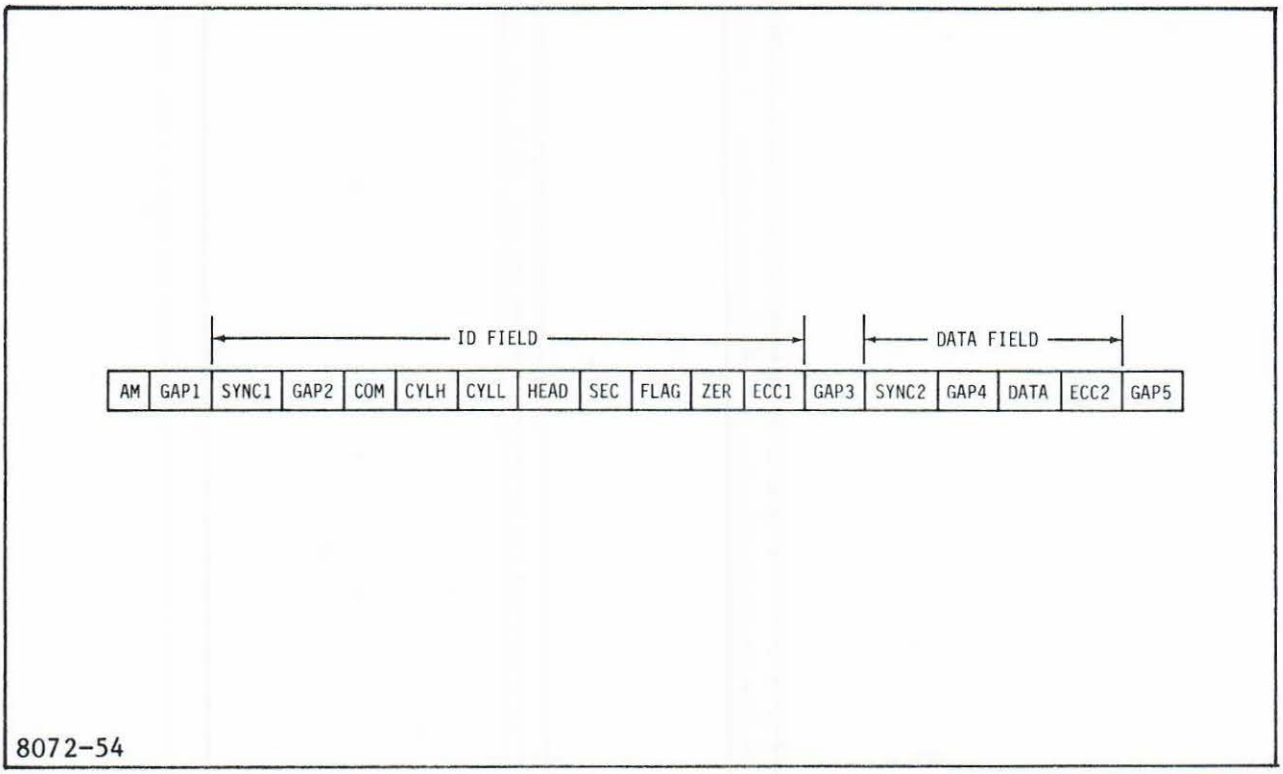


Figure 7-20. Sector Format

7.4 MAINTENANCE

The following paragraphs provide information necessary for maintenance of the Disk Drive. Included are removal and replacement procedures for major sub-assemblies and a description of the built-in diagnostics. The Disk Drive requires no preventive maintenance and has no adjustments.

7.4.1 Diagnostics

The diagnostics are divided into three sections: 1) Power-up Diagnostics, 2) Operational Error, and 3) Fault Diagnostics.

7.4.1.1 Power-Up Diagnostics

During the power-up sequence in the drive, a number of automatic diagnostic routine sequences are performed before the drive becomes ready for system usage. When a fault occurs, an appropriate error code is displayed in the fault indicators. Table 7-17 lists the description of these tests and the applicable error code.

The Power On LED is used to flash error messages when fault conditions occur in the drive. A 4-bit binary code is used (long flash = logic 1 and short flash = logic 0) with the most significant bit occurring first. (e.g. short, short, long, long = 3 (0011).

Table 7-17. Power-Up Sequence Error Codes

ERROR CODE	ERROR
1(0001)	No index track data burst at track 2 or track 3
2(0010)	No flag 0 from track 0 detector
3(0011)	Motor speed exceeds $\pm$1% tolerance
5(0101)	Flag 0 always true
9(1001)	Microprocessor self-test failed
10(1010)	No Index
11(1011)	Motor not up to speed

The power-up sequence error codes are detailed in the following paragraphs.

Codes 9, 10 and 11 - The first check is a microprocessor self-test. A check sum is performed on all the code bytes, and failure results in the display of fault code 9. Following the self-test, the microprocessor checks for an Index pulse (Hall sensor output) from the dc motor. If this does not occur during a period of 8 seconds, then fault code 10 is displayed. Since this condition is likely to be the result of the dc motor not starting, the microprocessor attempts to reduce head/disk static friction (during a period of 8 seconds) by moving the positioner four times (one track in alternate directions).

The dc motor speed is then checked to determine if it is within 3600 rpm ±1%. Each check takes one motor revolution, and during this time the Power On LED is flashed at intervals of approximately 0.5 second. If the processor does not see four consecutive speed samples correct to ±1% within 25 seconds, it will display fault code 11.

Codes 5 and 2 - When the speed check is successfully completed, Write Fault interrupts are enabled. The microprocessor then begins the re-calibration of the actuator to track 00. Two possible fault codes may occur. If Flag 00 does not go false within 25 steps toward the center of the disk, fault code 5 will be displayed. After going false, if Flag 00 cannot then be set true within 512 steps in the out direction, fault code 2 is displayed.

Codes 1 and 3 - After calibrating the actuator to track 00, the processor initiates a routine to select the correct Index pulse. The actuator is moved to track -2 to find the index data burst on head 0 and to select the corresponding Hall sensor phase, thus establishing Index. This operation involves checking for the data burst on track -3 if it cannot be located in track -2. Failure to complete this operation results in fault code 1 if link B is present and does not if link B is cut. The actuator is then re-positioned on track 00, and a final check made on the dc motor speed. If it is not within ±1% tolerance, fault code 3 is displayed.

At the successful completion of the power-up routine, Ready and Track 00 are both set true and the head selects are enabled.

7.4.1.2 Operational Error Check

During normal system usage and/or diagnostic self-testing, a number of built-in self-tests are perfromed. If any error conditions are detected by the micro-processor, an error code is displayed by the Power On LED indicator. Table 7-18 lists the tests and the applicable error codes.

Table 7-18. Operational Error Codes

ERROR CODE	ERROR DESCRIPTION
4(0100)	Motor speed exceeds +10%, -5% tolerance during normal operation
6(0110)	Step pulse while Write Gate is true
7(0111)	Static Write Fault condition: 1. Write current and no Write Gate, or 2. No write current, no Write Gate, or 3. More than one read/write head selected, or 4. 12-volt supply below 10.3 volts, or 5. 5-volt supply below 4.5 volts

The operational error codes are detailed in the following paragraphs.

Codes 4 and 6 - While the processor is waiting for a step pulse from the interface, it continuously monitors the dc motor speed. Should the speed vary from nominal by more than +10% or -5%, fault code 4 will be displayed. The processor will not allow a step pulse to be received while Write Gate is true. This is considered to be a catastrophic controller fault. The drive returns to Write Gate status and displays fault code 6.

Code 7 - On receipt of a Write Fault interrupt from the drive's hardware detection circuitry, the processor latches this condition, delays for 2 seconds and samples the hardware input to check if the Write Fault condition still exists. If it does, fault code 7 is displayed. If not, the processor enters the power-up routine thus setting the actuator to track 00.

7.4.1.3 Fault Diagnostics

Table 7-19 shows the likely causes and corrective action for power-up sequence and operational faults. The simplest action is to remove and replace either the master electronics board or motor speed board and verify that the fault code persists.

Table 7-19. Fault Diagnostics

FAULT CODE	PROBABLE CAUSE	CORRECTIVE ACTION
1	Faulty flag 00 position	Contact service organization
	Fault in data burst detection circuitry	Replace master board
	Fault in head 0 or preamp board	Contact service organization or replace preamp board
2,5	Transit lock label not removed	Remove
	Connector fault between motor speed board and stepper motor/ flag 00 assembly	Check connector and/or replace board
	Short circuit between motor speed board and casting	Reassembly board
	Faulty flag 00 transducer	Contact service organization
	Fault in stepper motor control circuitry	Replace master board or motor speed board
	Faulty stepper motor	Contact service organization
	Defective positioner assembly	Contact service organization
3,4	Brake failure	Replace
10,11	No 12V supply	Check supply/connector
	Faulty dc motor/Hall element	Contact service organization
	Faulty motor speed board	Replace
6	Controller/Interface fault	Check controller/connector
	Faulty master board	Replace
7	Faulty master board	Replace
	Faulty preamp board	Replace
	5V and/or 12V too low	Check supply
9	Faulty microprocessor	Replace master board

In practice, however, the most likely sources of trouble are (a) power supplies out of tolerance, and (b) step rates out of the drive constraints. In any event, the following should be verified:

1. The connectors are clean and properly attached.

2. The interface terminator is present, or absent, according to the configuration.

3. Link A is removed for the 3.1 milliseconds to 8.0 milliseconds range.

4. The drive chassis is free of any system metalwork.

5. The dc power lines are short-twisted pairs.

6. Data and control cables are properly shielded and do not run close to high current switching circuits.

7.5 Removal and Replacement Procedures

The following paragraphs detail the removal and replacement procedures for the major subassemblies. Be sure to read each procedure before attempting removal or replacement.

There is no preventive maintenance, and there are no adjustments on the drive. Field repair is restricted to replacement of Power Supply PCBA, Disk Controller PCBA, Master Electronic PCBA, Motor Control Board, Brake Assembly, and Head Disk Assembly.

NOTE

Repair to the HDA can only be effected by the use of Ampex special tooling and Class 100 clean-room conditions.

The tools required for field repair consist of the following:

a. Pozidrive screwdriver, No. 2.

b. Phillips head screwdriver, medium.

c. Hex driver, Allen, 5/64 inch.

d. Slot screwdriver, medium.

7.5.1 Disk Assembly Top Cover Removal and Replacement

1. Remove power cord and interface cable from the rear of the Disk Drive.

2. Remove two (2) screws on the rear of the Disk Assembly chassis. See figure 7-21 (A). The top cover can now be removed by sliding the cover forward from the chassis track.

3. Replace the top cover by sliding the back of the cover onto the front of the chassis, aligning the cover track rail with the chassis.

4. Replace two (2) screws from the rear of the chasssis. See figure 7-21 (A).

7.5.2 Disk Controller Board Removal and Replacement

1. Remove Disk Drive top cover (refer to paragraph 7.5.1).

2. Remove the four cable connection from the controller board (P2 Host, P1 Power, J1 Drive Control, and J3 Drive Data). See figure 7-21 (B).

3. Using a flat object (screwdriver or letter opener) depress the locking tabs on the four mounting studs and remove controller board. (See figure 7-22.)

4. To replace controller board, position the four mounting studs through the mounting holes on the controller. Ensure that each mounting stud locking tab engages. Replace the four cables removed in step 2 above.

7.5.3 Power Supply Removal and Replacement

1. Remove Disk Drive top cover (refer to paragraph 7.5.1).

2. Remove power supply cable P1.

3. Using a flat object (screwdriver or letter opener) depress the locking tabs on the four mounting studs and remove the power supply board. (See figure 7-22.)

4. To replace the power supply board, position the four mounting studs through the mounting holes on the power supply. Ensure that each mounting stud locking tab engages. Replace the power cable removed in step 2 above.

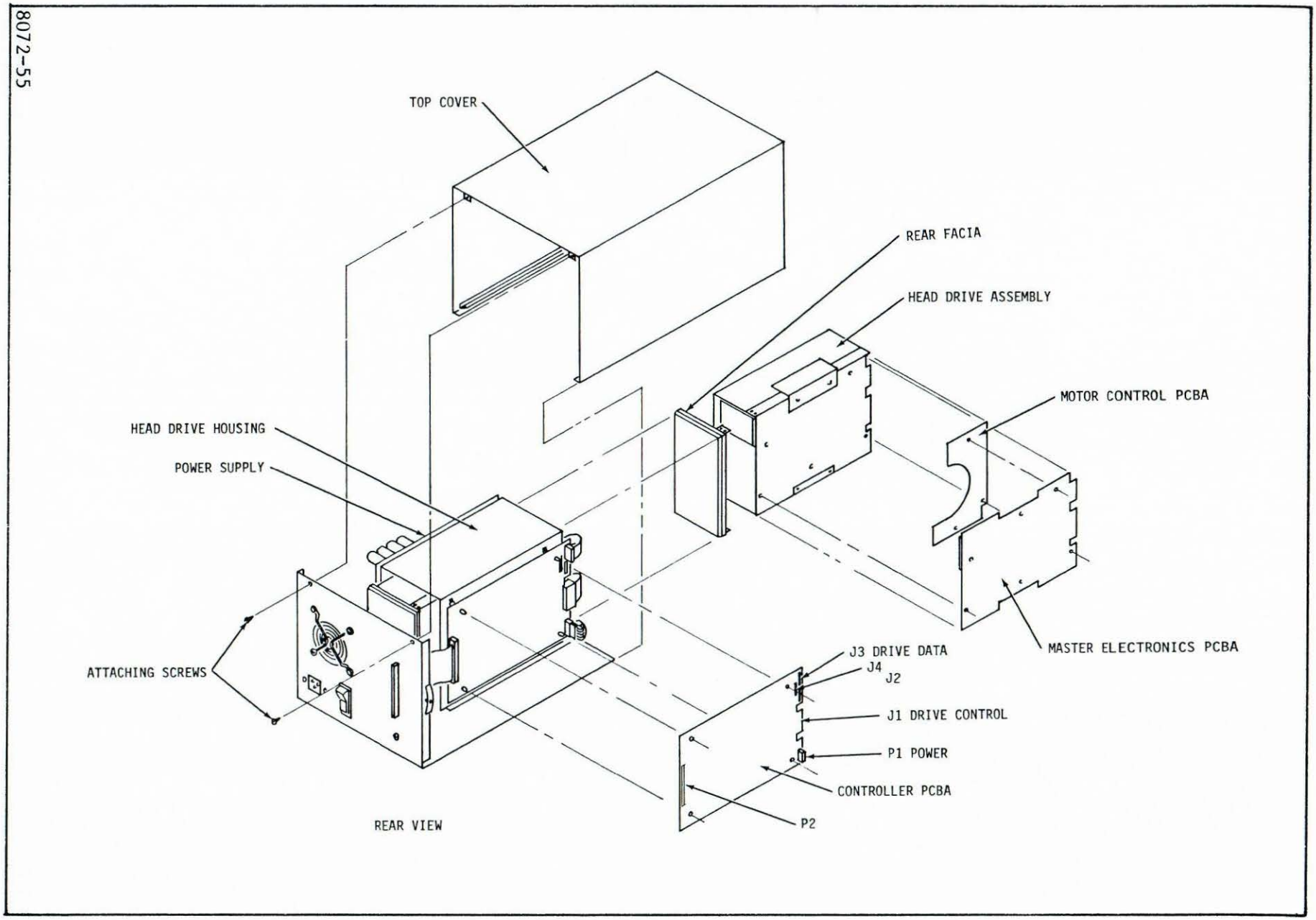


Figure 7-21. Disk Drive Disassembly

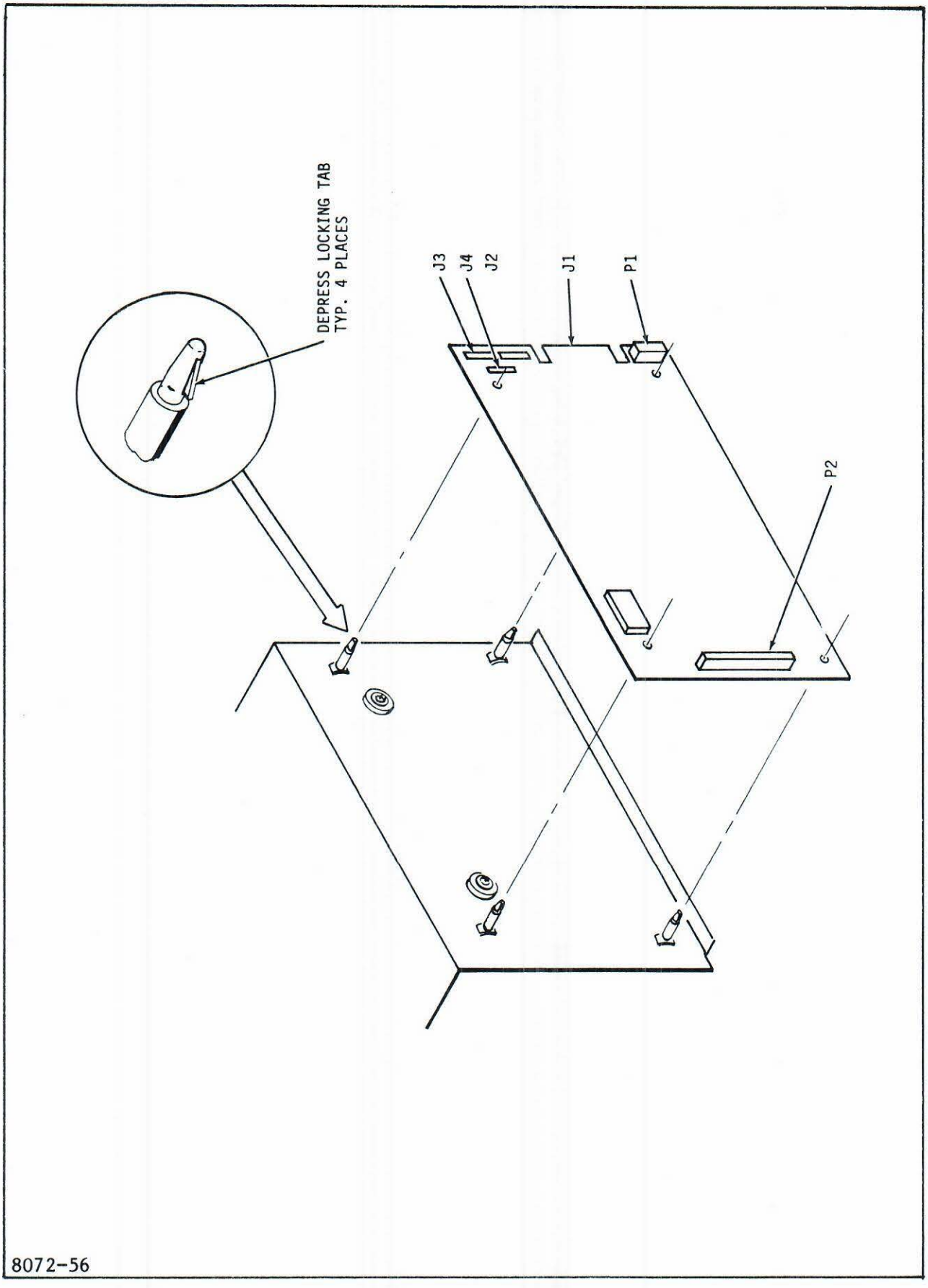


Figure 7-22. Controller PCBA Removal

7.5.4 Disk Drive Assembly Removal and Replacement

1. Remove Disk Drive top cover. (Refer to paragraph 7.5.1).

2. Remove the four cable connections from the Disk Assembly (J1 Drive Data, J3 Drive Control, P2 Power, Groung Lug). See figure 7-23.

3. Remove the controller board (Refer to paragraph 7.5.2).

NOTE

Before removing drive assembly shock mounting screws, support the bottom of the drive with a 1/2 inch support block (a folded piece of cardboard or similar).

4. Remove the two shock mounting screws (Phillips Head) located on the left side of the Drive housing (under the controller board).

5. Carefully support the drive assembly and remove the two shock mounting screws (phillips head) located on the right side of the drive housing (below power supply board). See figure 7-23. Slide the Drive Assembly forward, out of the housing.

6. Remove the top mounting bracket (two (2) mounting screws) of the Drive Assembly is to be replaced.

7. To replace the Drive Assembly, reverse the above procedure.

7.5.5 Master Electronic Board Removal and Replacement

1. Remove Disk Drive top cover. (Refer to paragraph 7.5.1).

2. Remove Disk Drive Assembly. (Refer to paragraph 7.5.4).

3. Remove top mounting bracket from top of Drive Assembly.

4. Remove rear facia by removing two top and two bottom mounting screws (phillips head). See figure 7-24.

5. Using the Allen hex driver, remove the six screws securing the board to the drive. Carefully loosen connector J4 from the preamplifier board and lift the master board free from the drive.

6. Disconnect flat cable connector J5 from the motor speed control board.

7. To replace the master electronics PCBA, connect flat cable connector J5 to the motor speed control board, ensuring that the connector is properly polarized.

8. Ensure that connector J4 mates properly with the preamplifier board.

9. Secure the master electronics board to the drive with six screws.

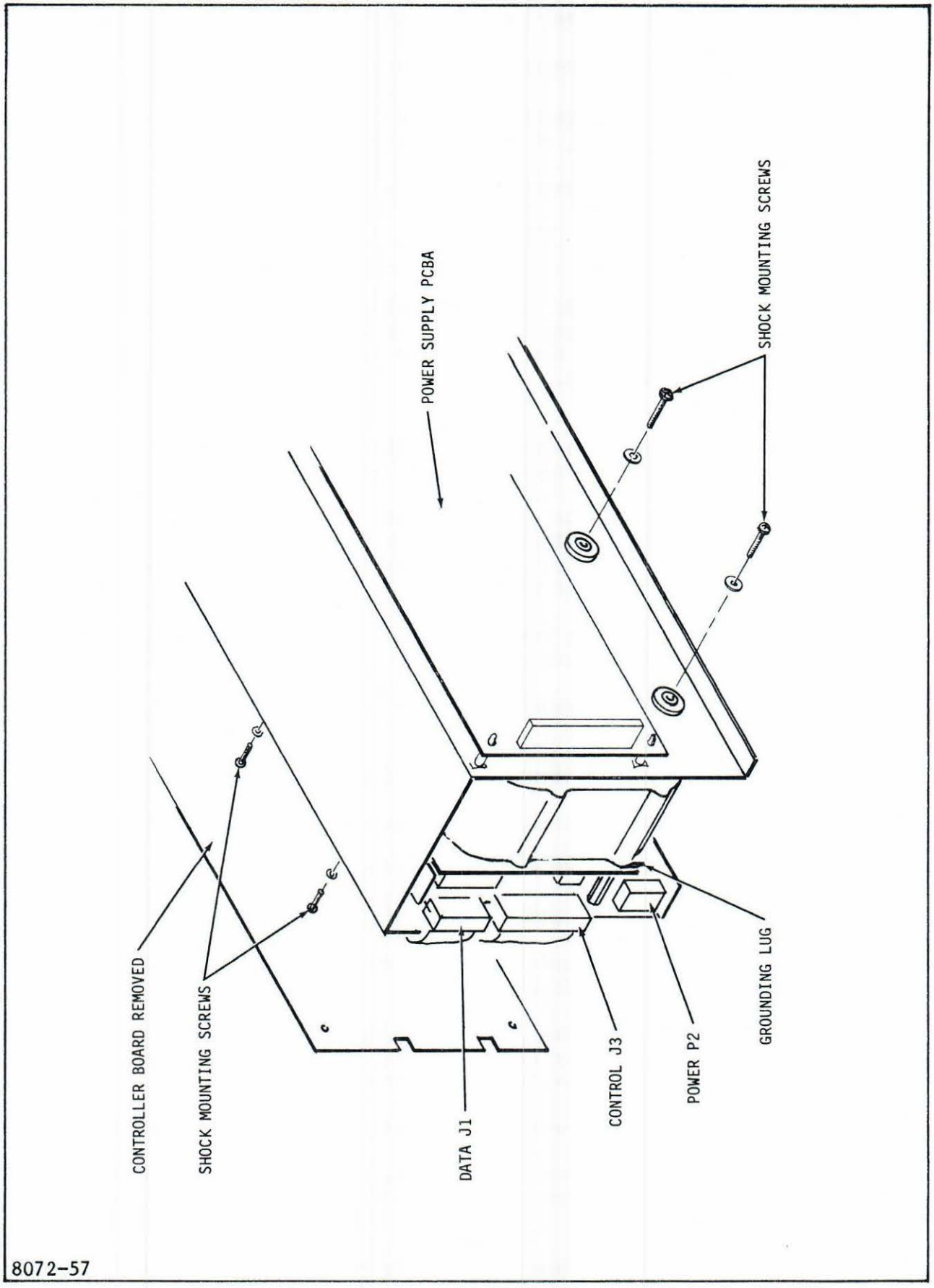


Figure 7-23. Head Drive Assembly Removal

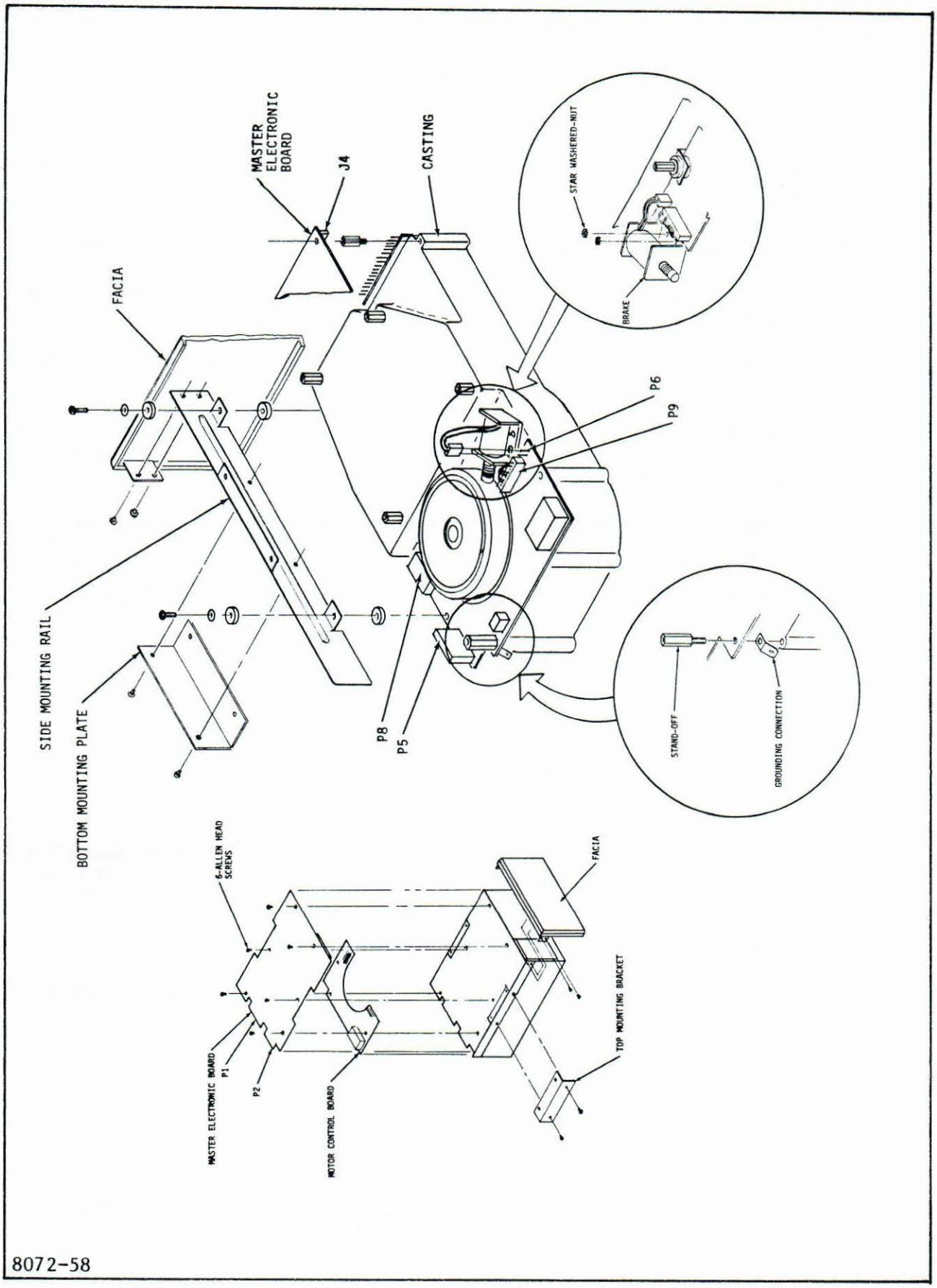


Figure 7-24. Head Drive Disassembly

7.5.6 Brake Removal and Replacement

1. Remove Disk Drive top cover. (Refer tp paragraph 7.5.1).
2. Remove Disk Drive Assembly. (Refer to paragraph 7.5.4).
3. Remove the master electronics board as described in paragraph 7.5.5 from the motor speed control board.
4. Disconnect brake connector J6 from the motor speed control board.
5. Using the box spanner, remove the two nuts securing the brake to the casting and remove the brake.
6. To replace the brake, position the replacement brake, and refit the nuts loosely.
7. Place the feeler gauge between the motor rotor and the brake pad, and push the brake body so that the plunger is fully depressed against its spring.
8. Ensure that the center line of the brake lines up with the motor center, and lock the nuts.
9. Reconnect the power connector, ensuring correct polarization.

WARNING

Before powering up the drive, make sure the motor is free of obstructions. Do not touch the spinning motor.

10. Power up the drive with the master electronics board lying alongside, and verify that the brake does not contact the motor rotor. Ensure that the master electronics board is isolated from metallic parts.
11. Power off and verify that stopping time is within 5 to 8 seconds.
12. Refit the master electronics board as described in paragraph 7.5.5.

7.5.7 Motor Control Board Removal

1. Remove the master electronics board as described in paragraph 7.5.5.
2. Remove the screw securing the left mounting bracket to the casting.
3. Disconnect brake connector J6, dc motor connector J9 and stepper motor connector J8 from the motor speed control board.
4. Unscrew both the rear standoff with ground tab and left standoff; remove the motor speed board.
5. If the spare Hall element is to be connected, remove the link on the motor speed board and reconnect it as shown on the Motor Speed Control PWBA Assembly Drawing.
6. To replace the Motor Control PCBA, install the replacement motor speed board, insert the ground tab and tighten the rear standoff. Insert and tighten the left standoff.
7. Reconnect stepper motor connector J8, dc motor connector J9 and brake connector J6, ensuring correct polarization of the connectors.
8. Insert the screw securing the left mounting bracket to the casting.
9. Refit the master electronics board as described in paragraph 7.5.5.

7.5.8 Preamplifier Board Removal/Replacement

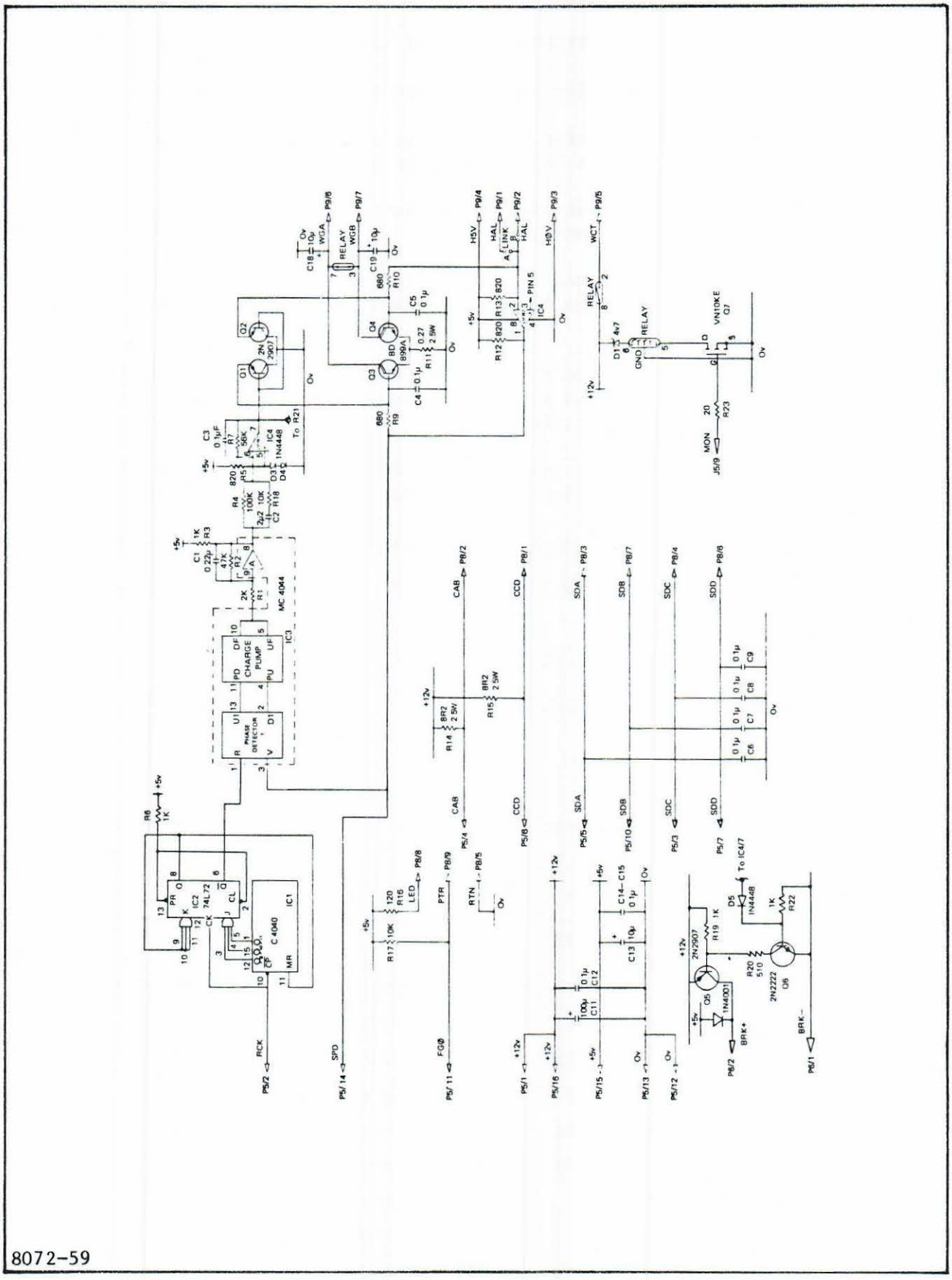
(Not recommended as field replaceable).

7.6 PARTS LIST

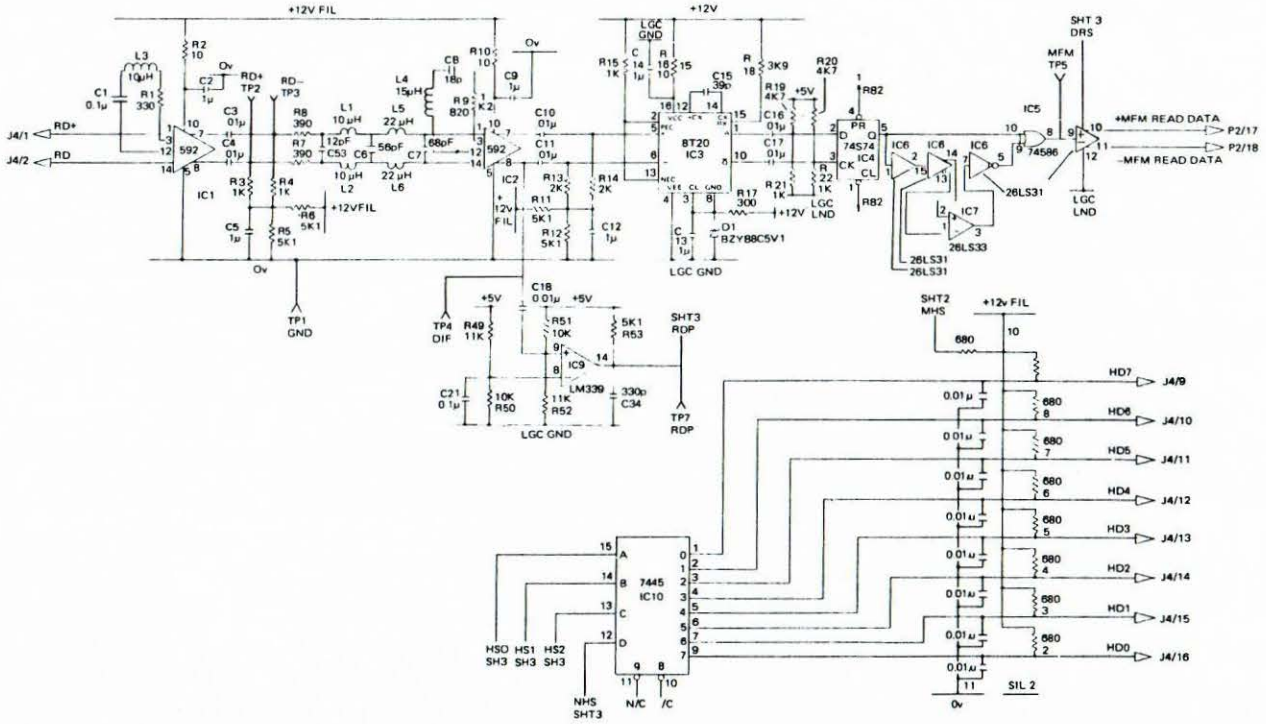
Table 7-20 is a listing of replaceable parts for replacing failed subassemblies.

Table 7-20. Parts List

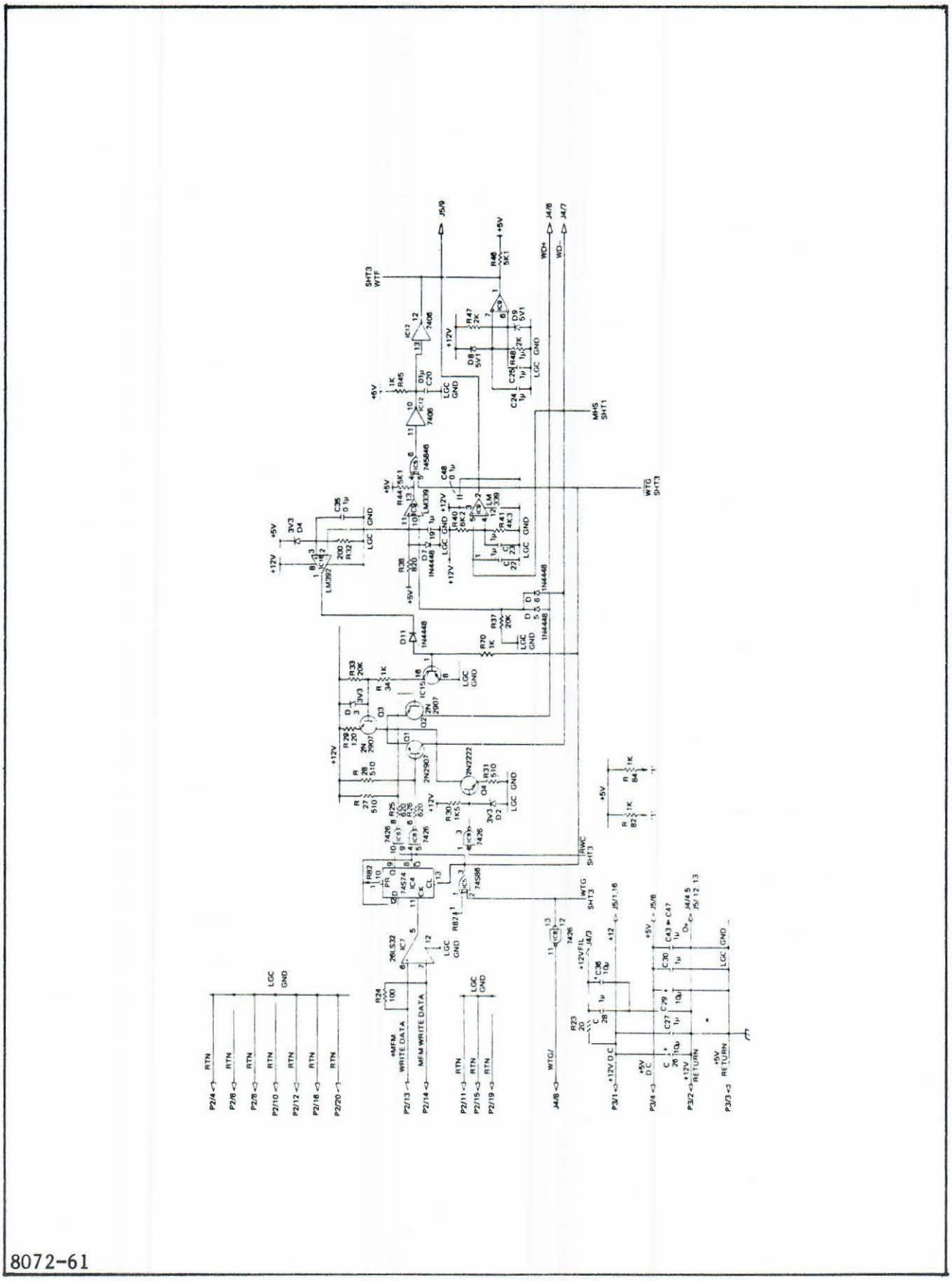
ICN	VENDOR PART NUMBER	DESCRIPTION
TT524090	400413-001	5-1/4 WINCH DISK DR. 10MB
TT524100	400413-002	5-1/4 WINCH DISK DR. 20MB
TT520080	903370-001	PCBA, WDD INTERFACE BOARD
TT520090	400444-001	PCBA, WDD CONTROLLER BOARD
TT520120	400446-001	PCBA, POWER SUPPLY
TT520100	ASY5023	PCBA, MASTER ELECTRONICS
TT520110	ASY5024	PCBA, MOTOR CONTROL
TT528160	TAB1004	GROUND TAB
TT528170	906608-001	CABLE, INTERFACE



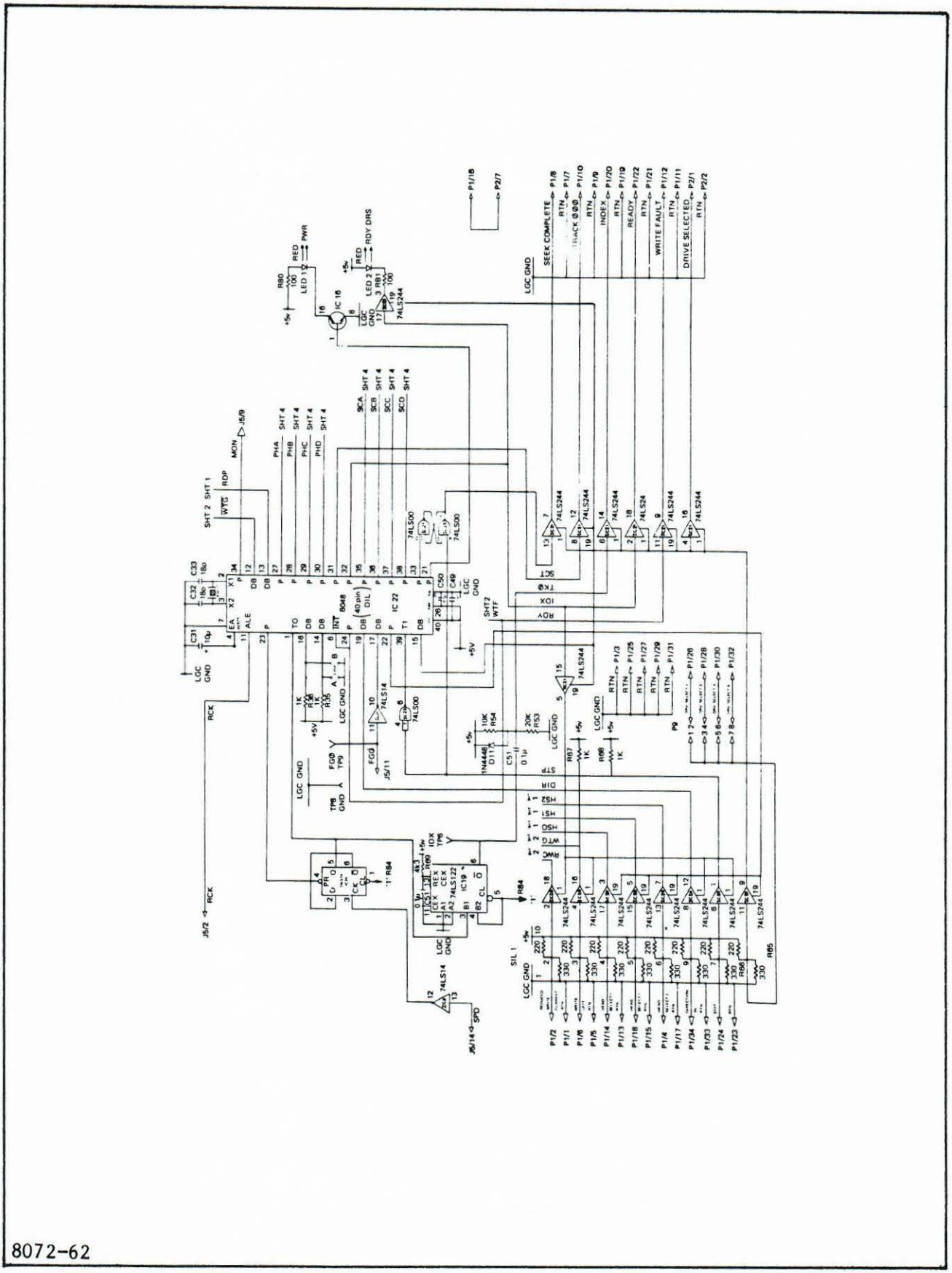
Motor Speed Control PCB Schematic



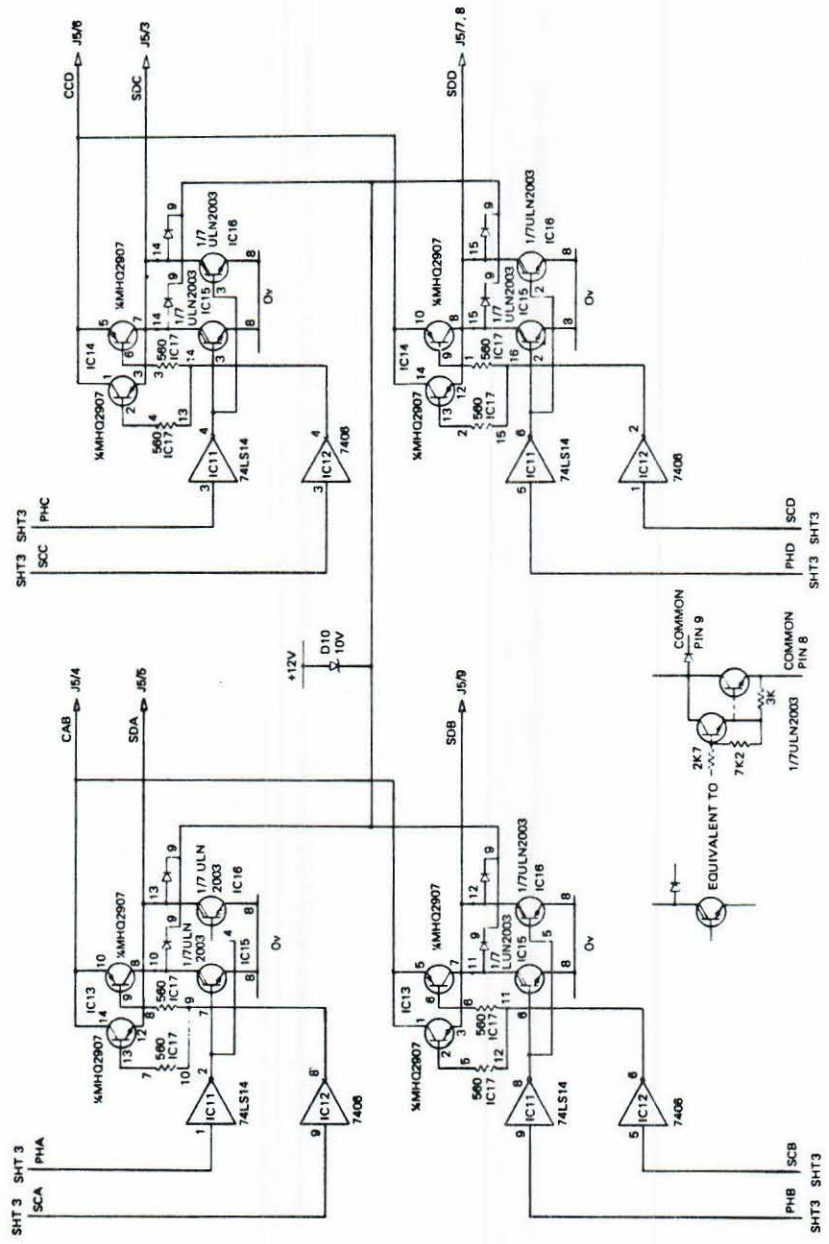
Master PCB Schematic (1 of 4)



Master PCB Schematic (2 of 4)



Master PCB Schematic (3 of 4)



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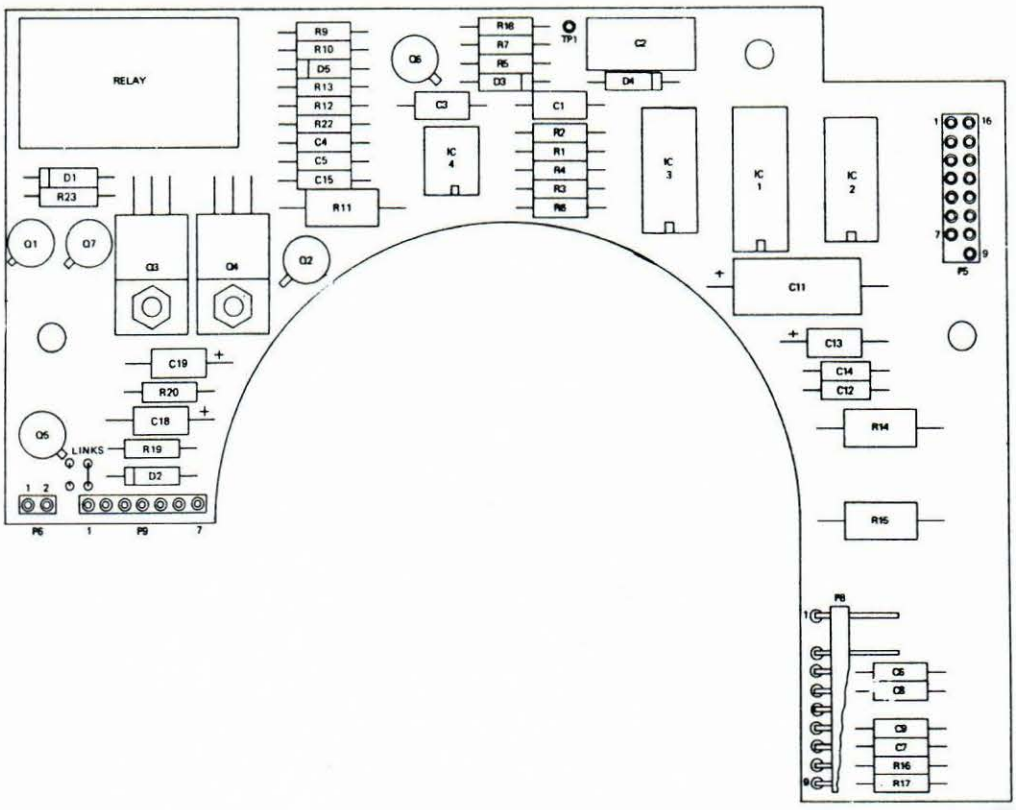
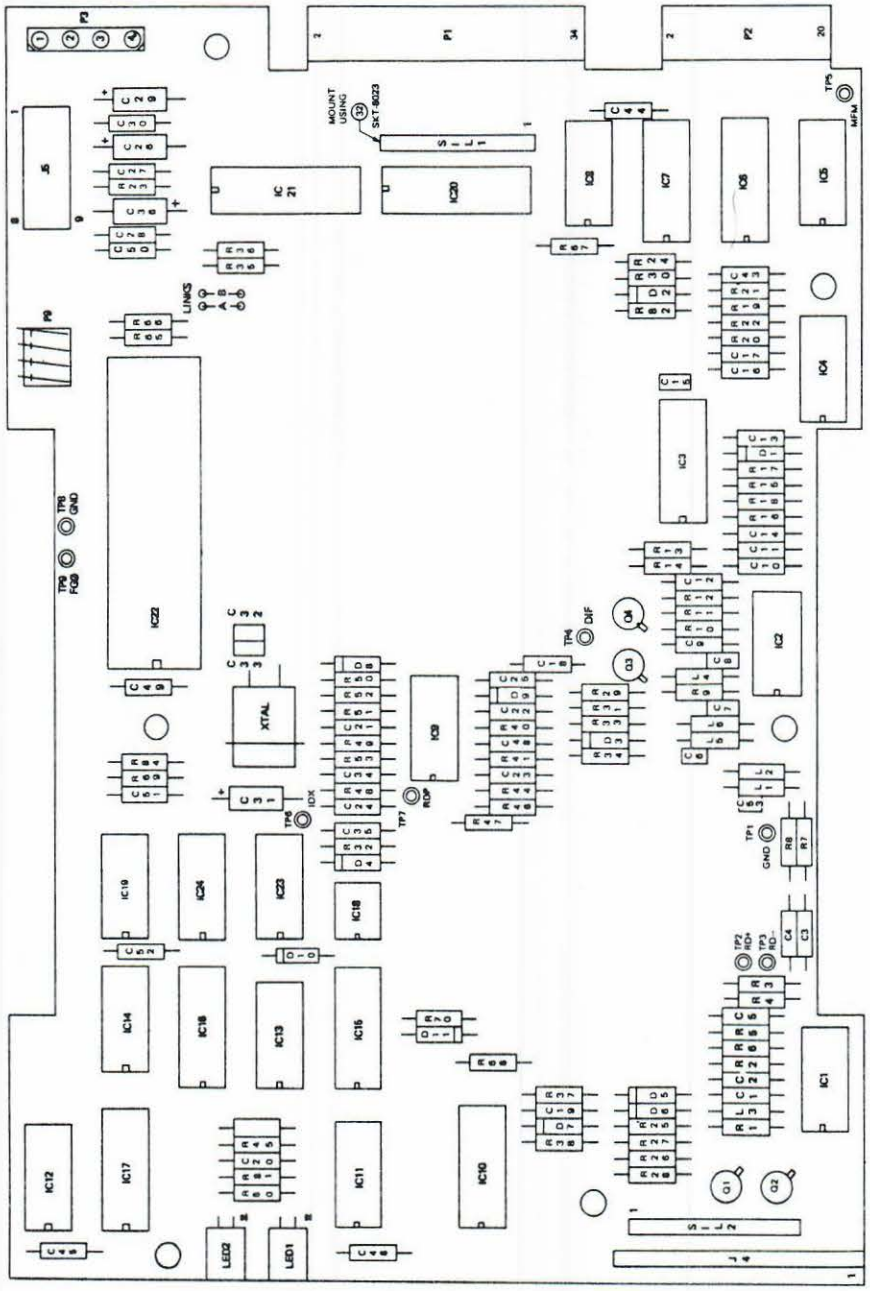
Master PCB Schematic (4 of 4)



8072-64

Motor Speed Control PCB Layout



8072-65

Master PCB Layout

SECTION VIII

REFERENCE DATA

This section provides schematics and other reference data for the Office Display Terminal (ODT) and System S/10.

Advanced Video Processor Schematic (S/10 - ODT)

Advanced Floppy Disk Controller Schematic

Power Supply Schematic (S/10 only)

Power Supply Schematic (ODT only)

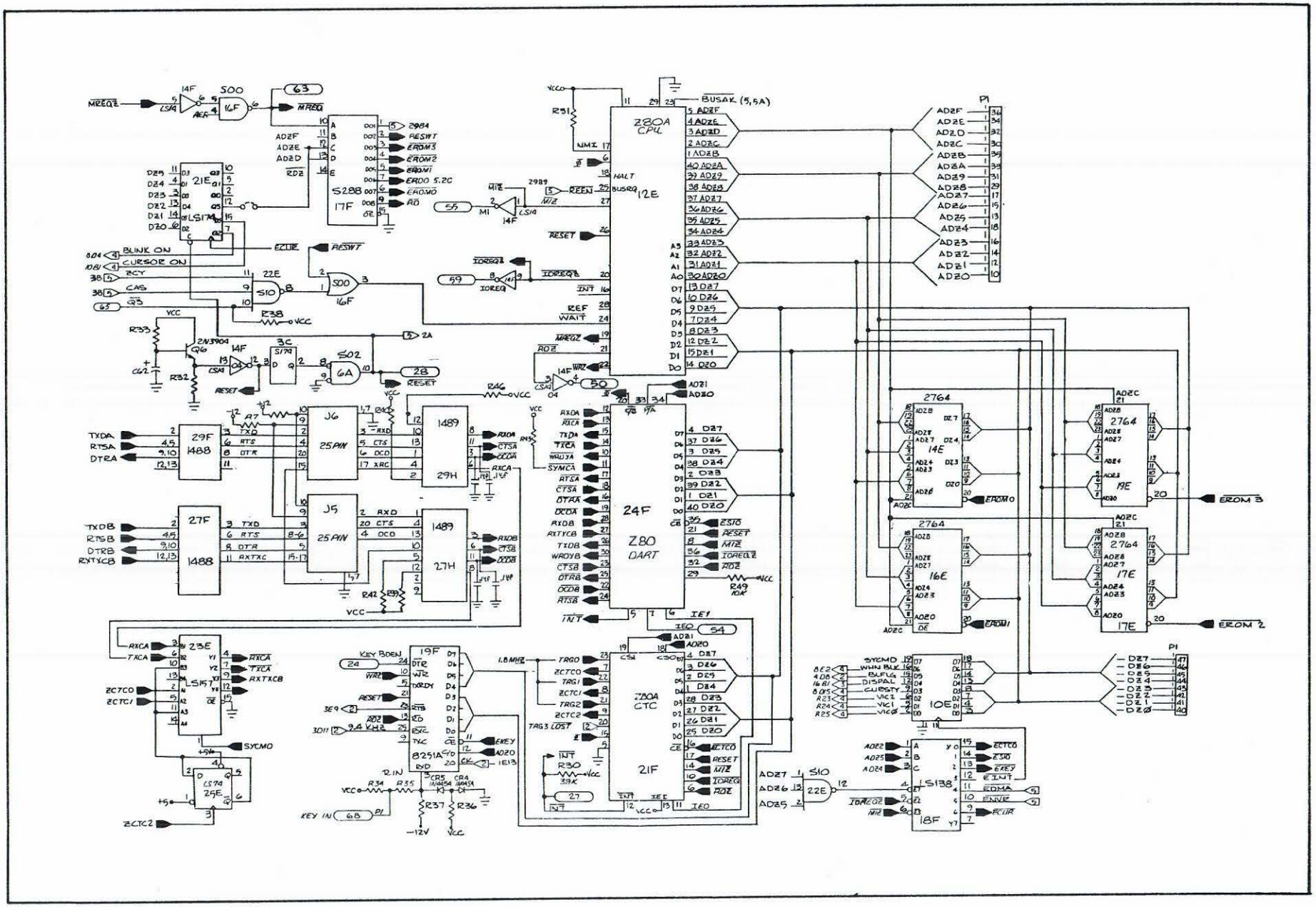
System S/10 Wiring Diagram

Disk Drive Schematic (S/10 Only)

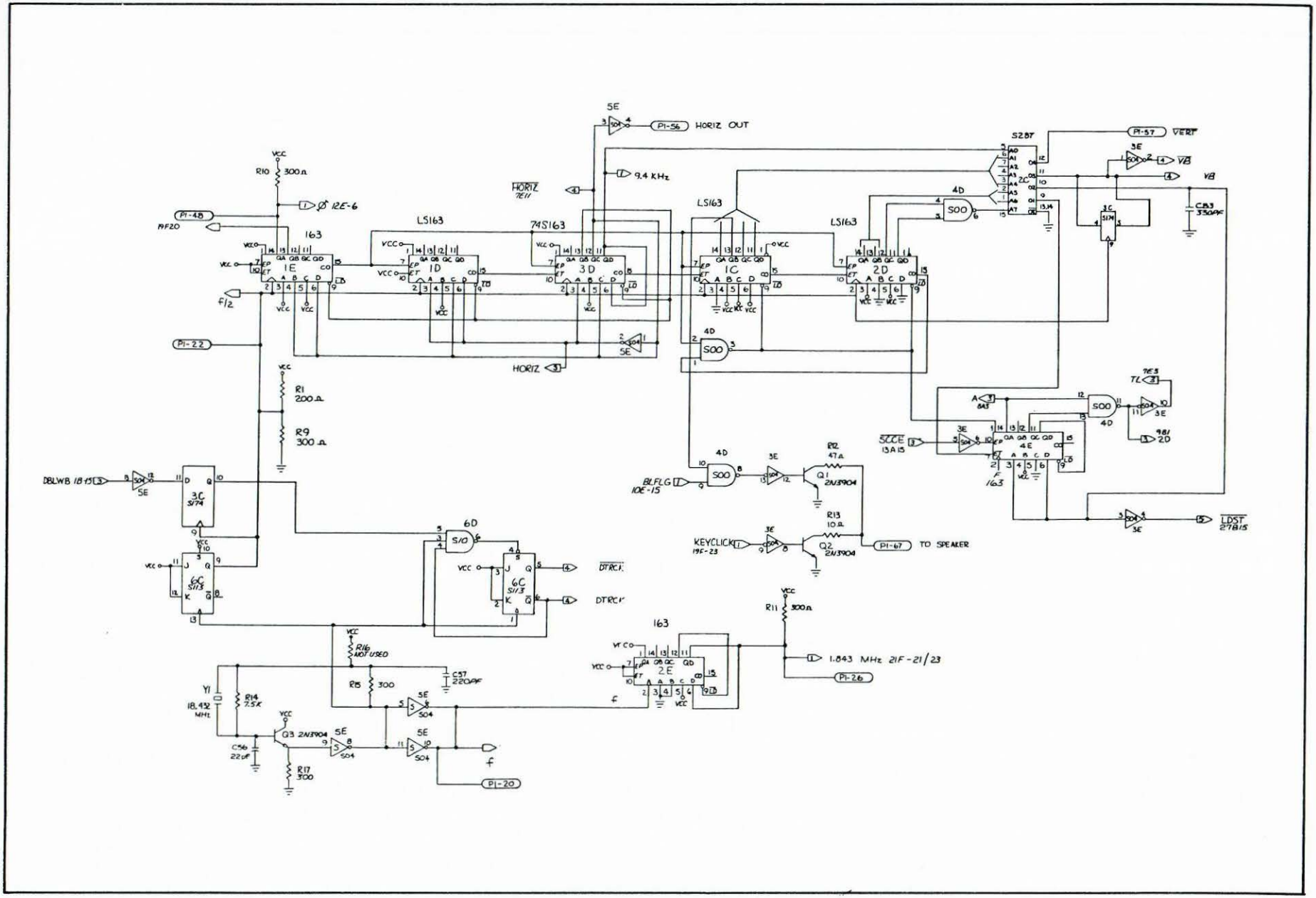
Printer Connection/Protocols and Auxiliary Pin Assignments

Table of ASCII Codes

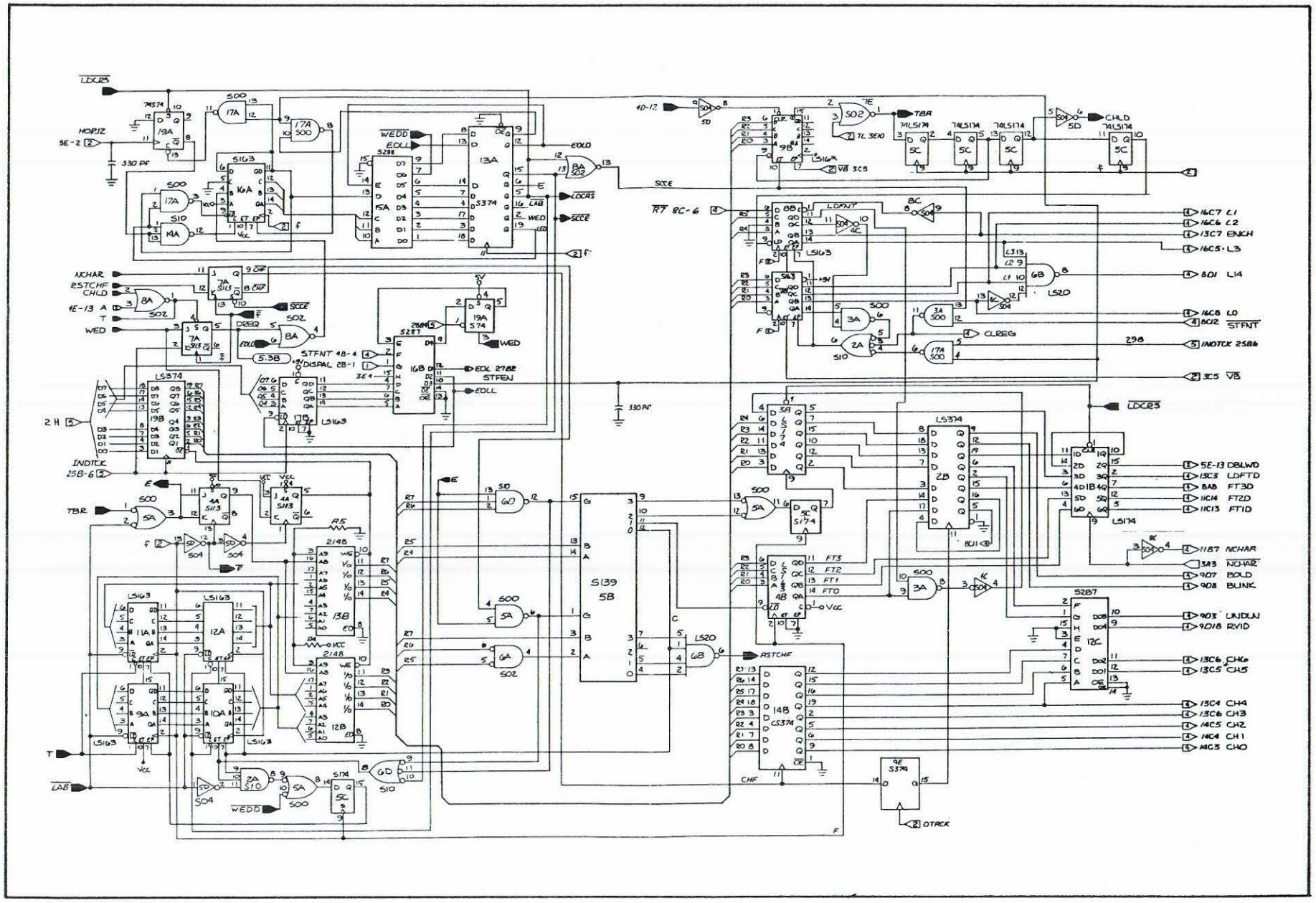
Glossary



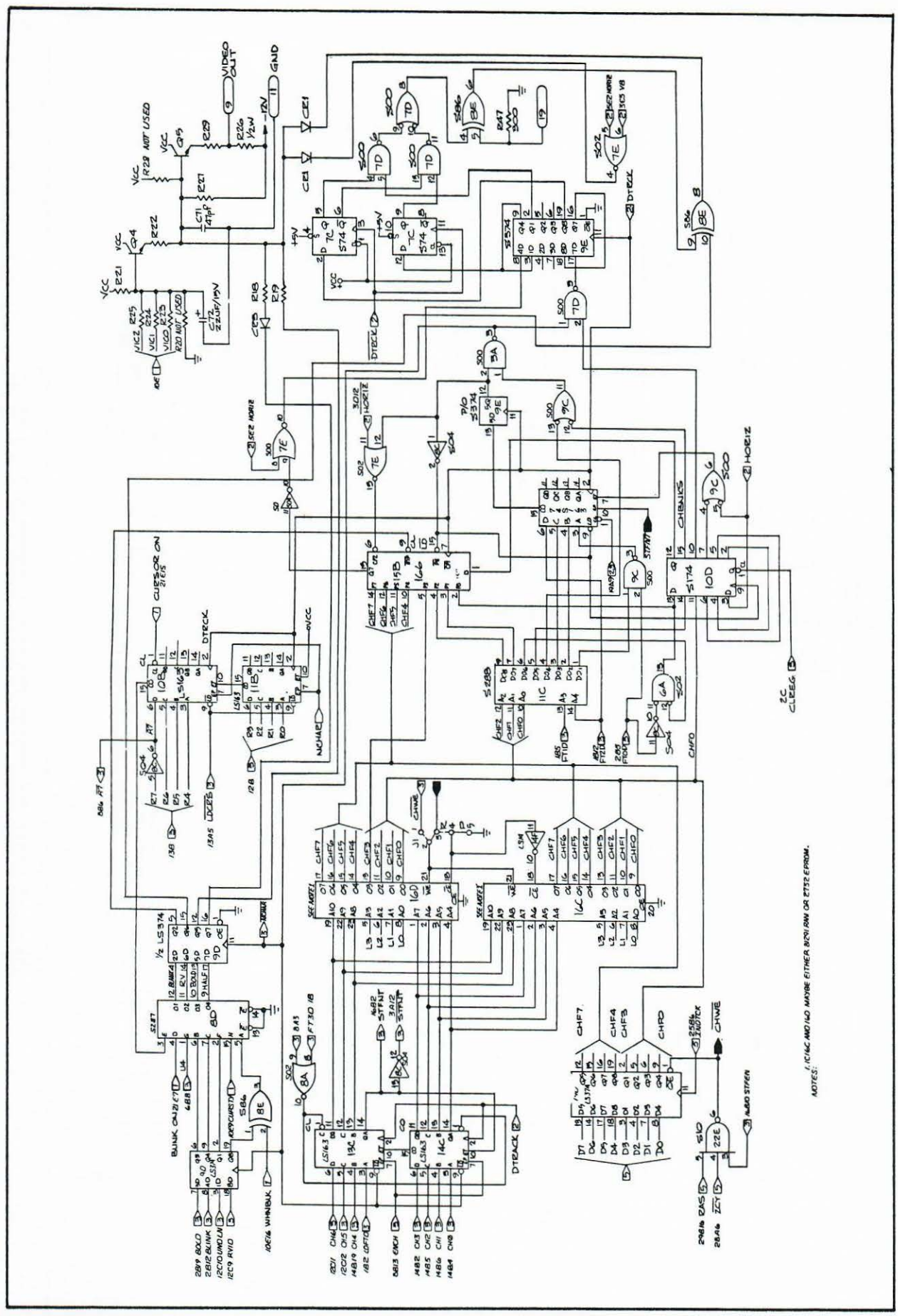
Advanced Video Processor Circuit Diagram AVP (1 of 5)



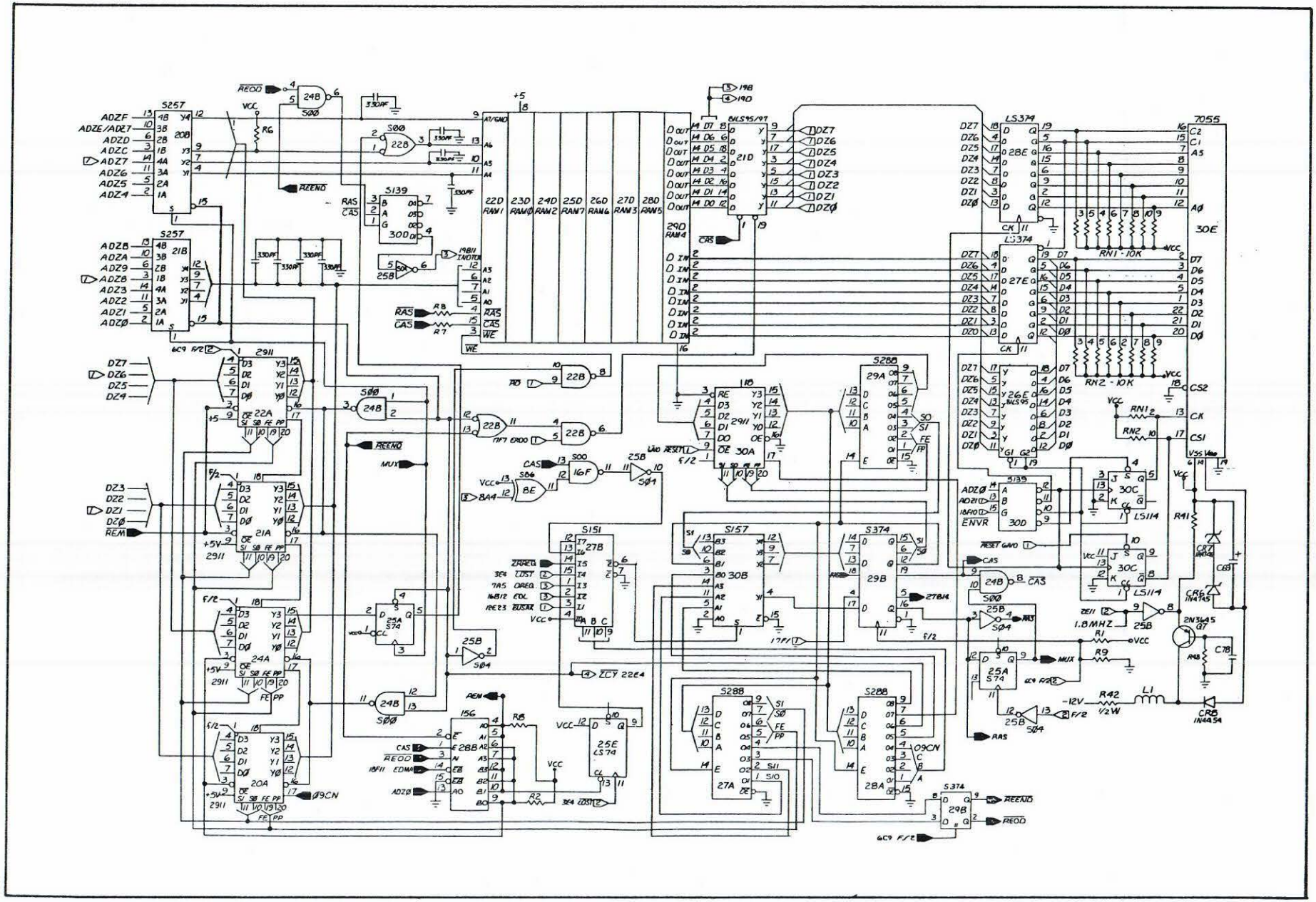
Advanced Video Processor Circuit Diagram AVP (2 of 5)



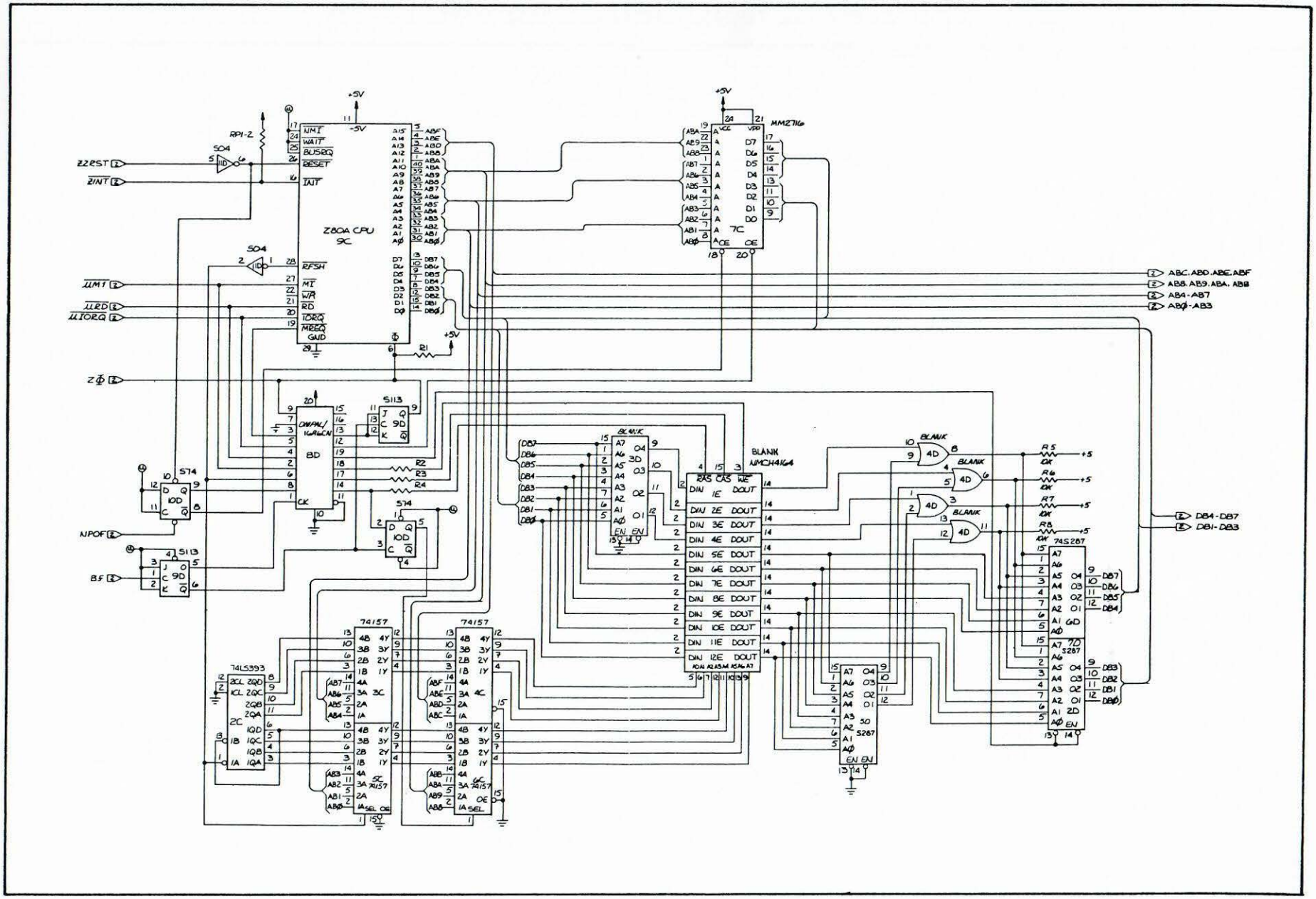
Advanced Video Processor Circuit Diagram AVP (3 of 5)



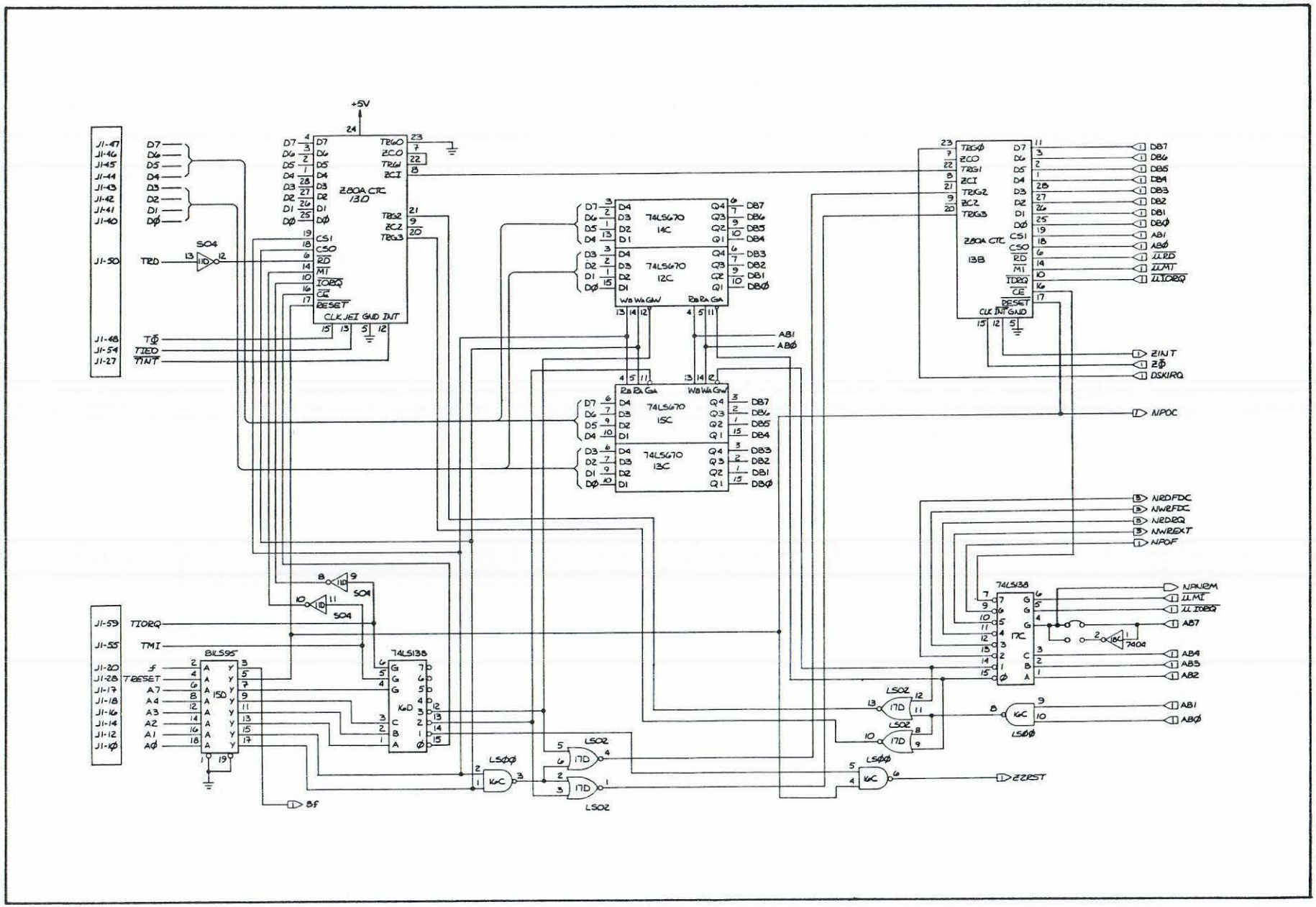
Advanced Video Processor Circuit Diagram AVP (4 of 5)



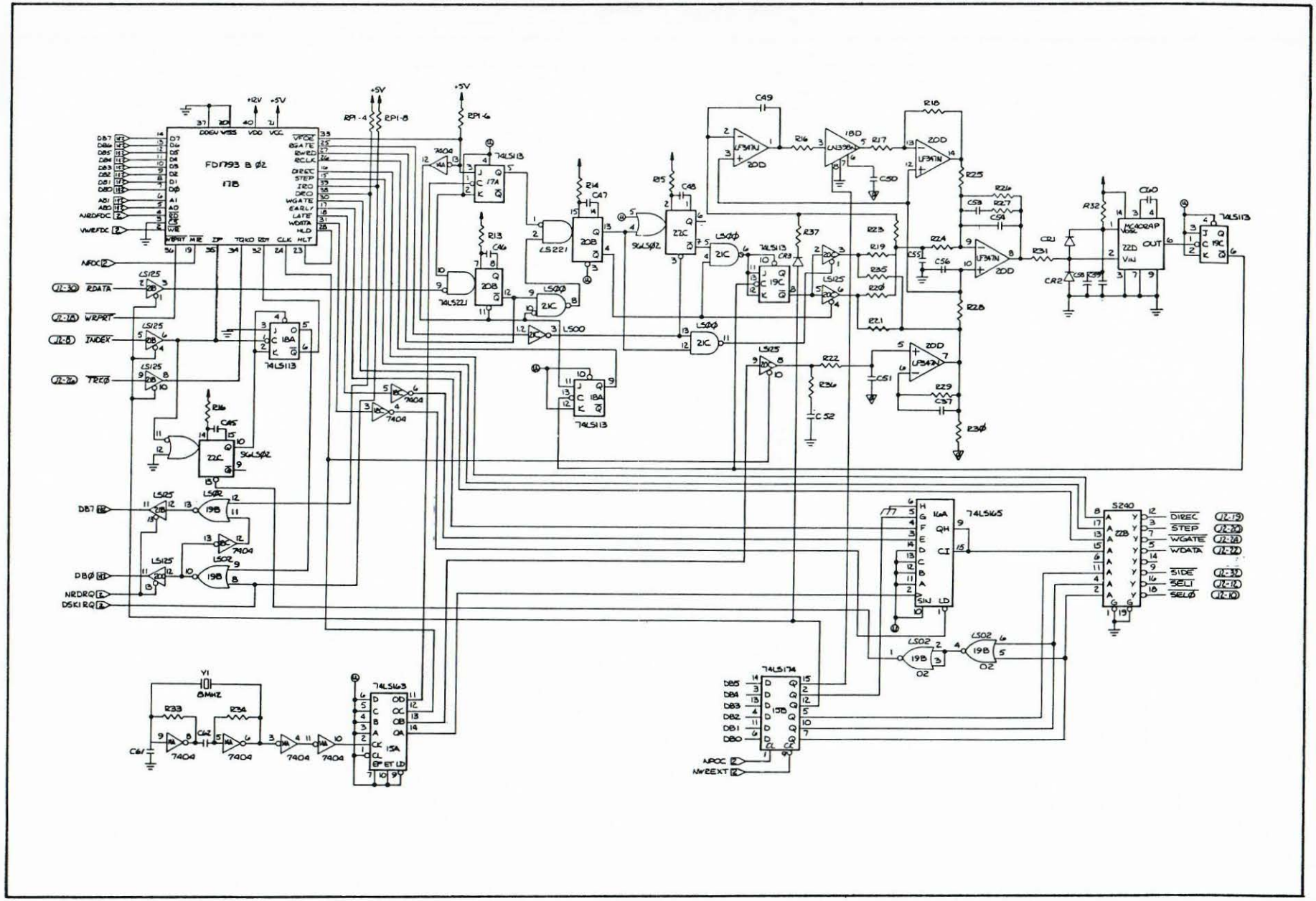
Advanced Video Processor Circuit Diagram AVP (5 of 5)



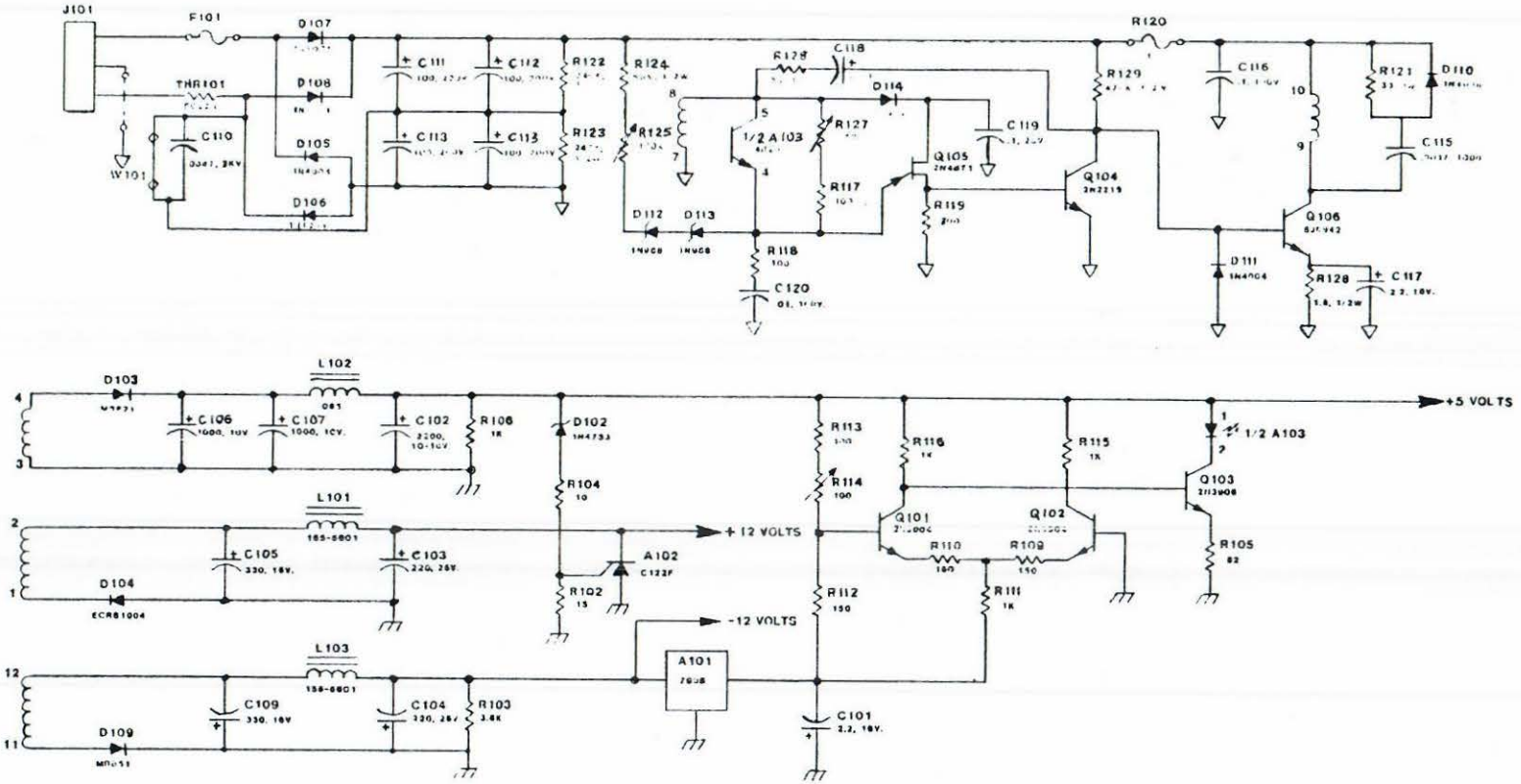
Advanced Floppy Disk Controller Circuit Diagram (1 of 3)



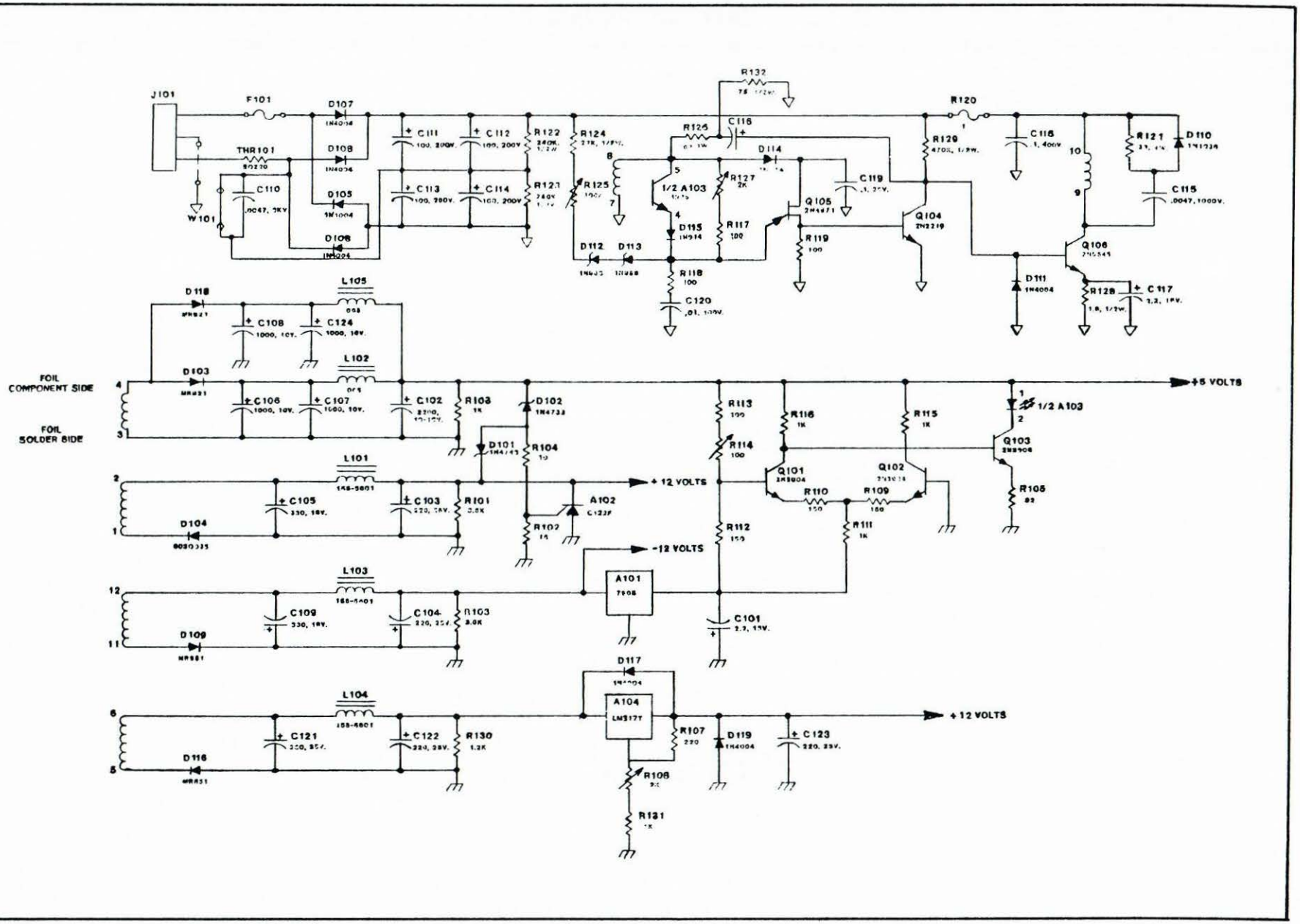
Advanced Floppy Disk Controller Circuit Diagram (2 of 3)



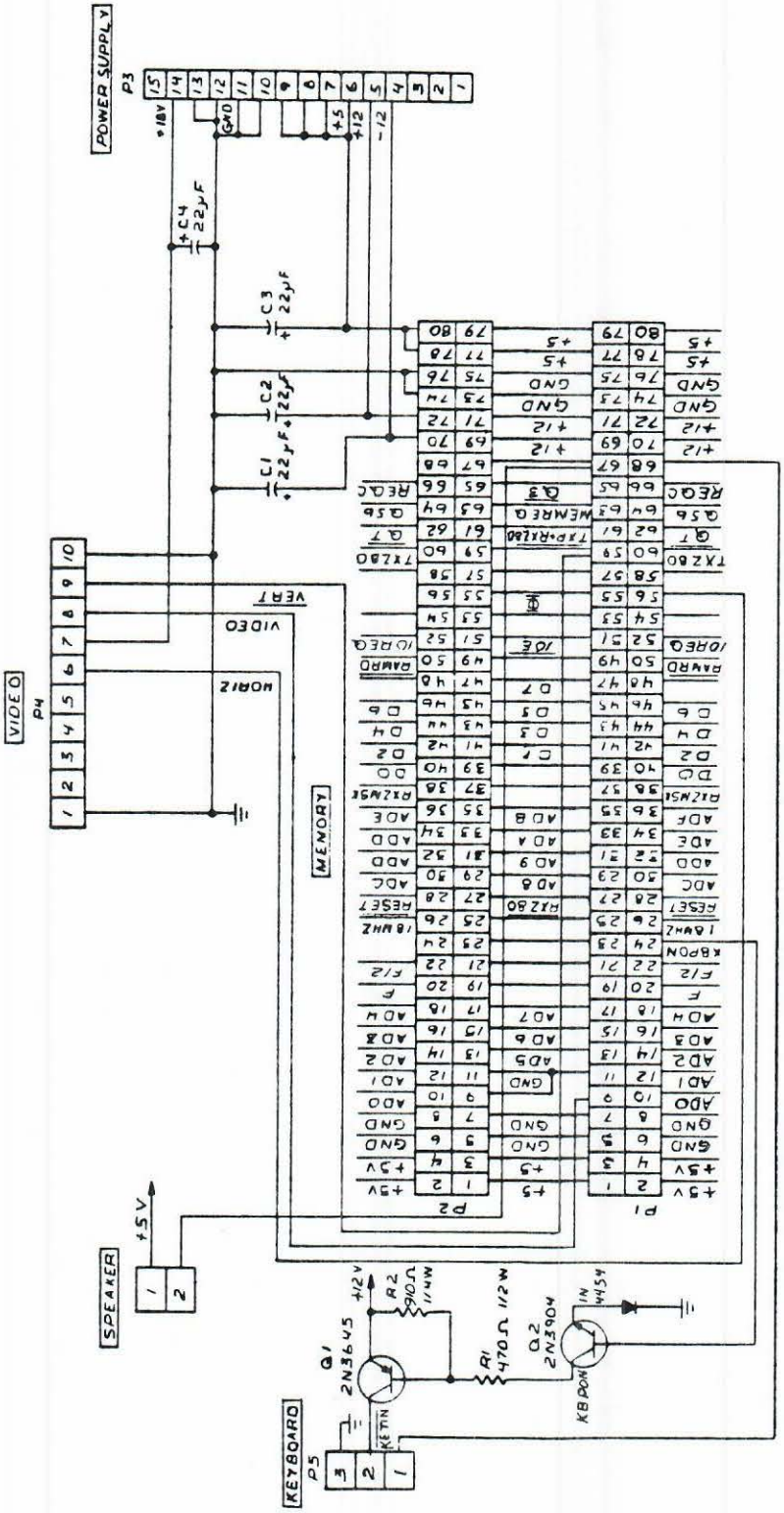
Advanced Floppy Disk Controller Circuit Diagram (3 of 3)



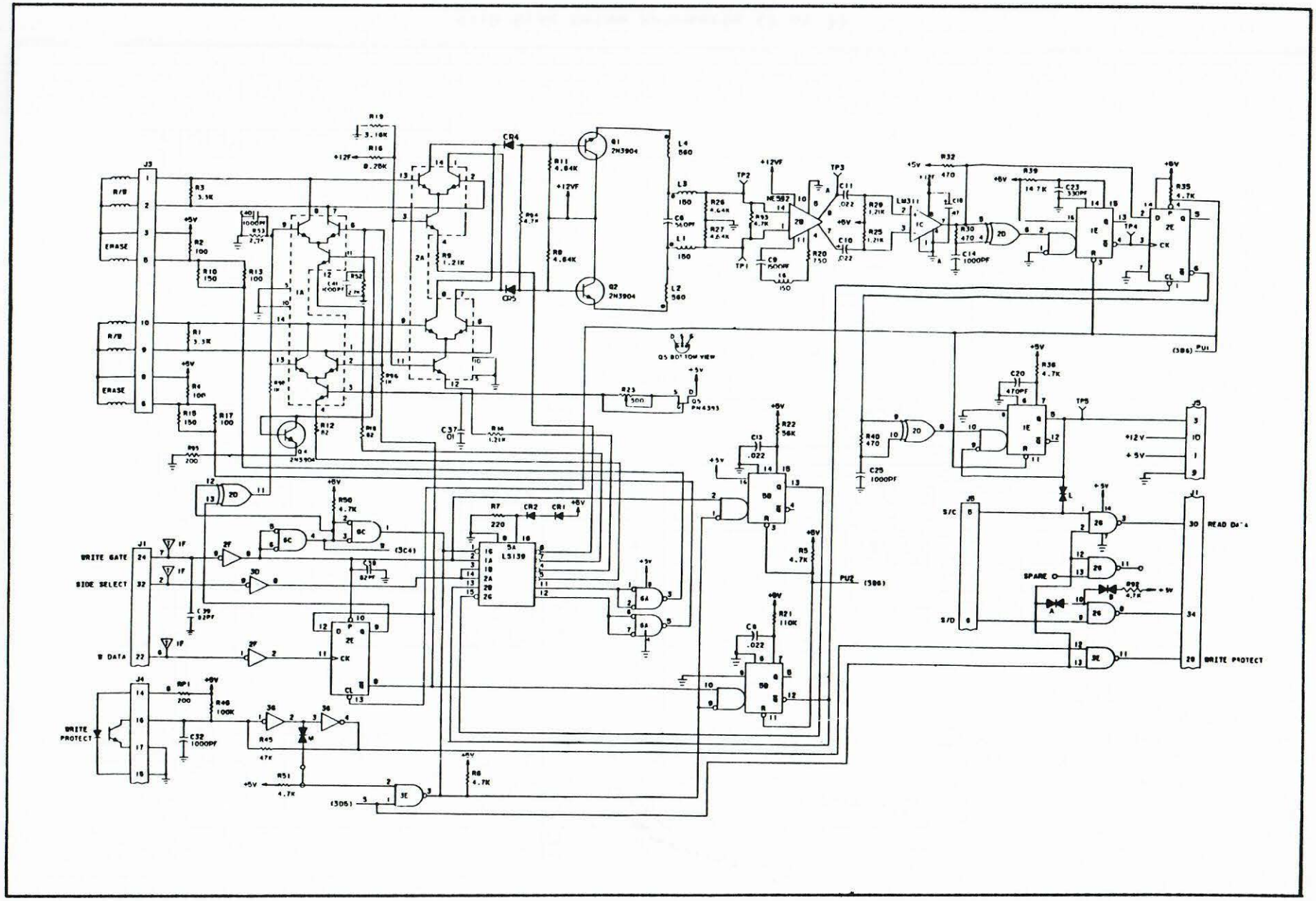
ODT Power Supply 90046 Rev. A



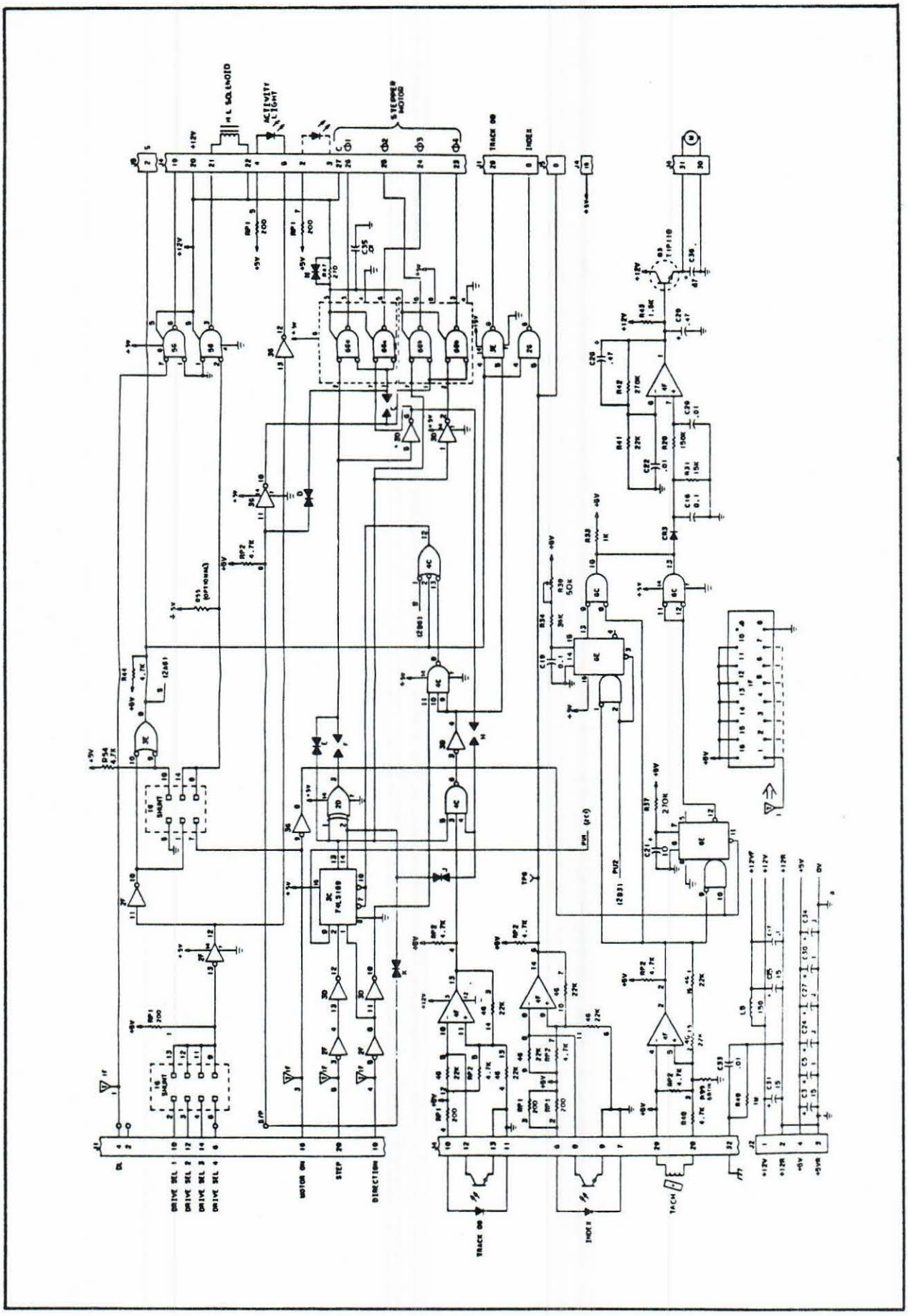
S/10 Power Supply 90045 Rev. A



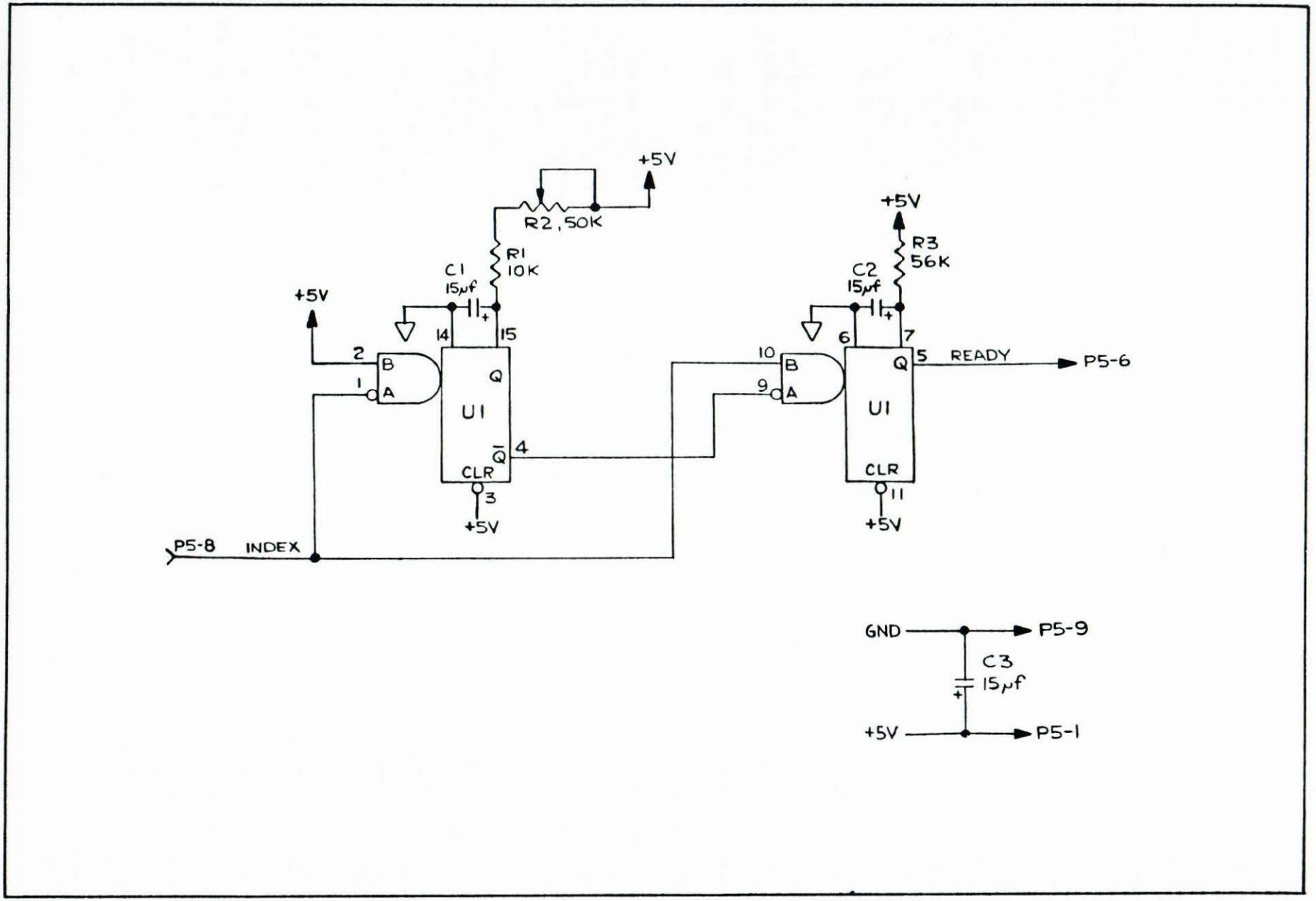
S/10 Wiring Diagram



S/10 Disk Drive Schematic (1 of 3)



S/10 Disk Drive Schematic (2 of 3)



S/10 Disk Drive Schematic (3 of 3)

PRINTER CONNECTON AND PROTOCOLS AND AUXILIARY PORT PIN ASSIGNMENTS

CONNECTION

Most ASCII printer models can be successfully used with the S/10 auxiliary port (to the left of the main port). The port is wired as a standard modem port and can be connected with a straight-through RS-232 cable.

PRINTER PROTOCOLS

When print is initiated, the S/10 outputs characters from the printer port to the printer's receive buffer (if it has one). Since the buffer is of finished length, the printer may not be able to accept and print characters as fast as the S/10 can transmit them, especially when it is transmitting at rates in excess of 600 baud. To prevent overrunning the receive buffer and loss of characters by the printer, the S/10 provides two control protocols, XON/XOFF processing and DTR Handhsake protocol. These protocols can be used individually or simultaneously.

The S/10 is capable of responding to XON and XOFF codes sent from the printer to stop and resume the transmission of data. This feature is set when field 1 of Status Line Three reads auto or both. The printer must be set up to generate these codes. These control codes have no effect if the unit is not set to recognize them. When both is displayed, both Auto XON/XOFF and DTR Handshake protocols are in effect.

If both the printer and the S/10 unit are properly set up, the printer sends an XOFF (DC3) to the S/10 when its receive buffer is nearly full. This signal causes the S/10 to stop transmitting characters. When most of the characters in the printer's receive buffer have been printed, the printer sends a XON (DC1) to the S/10, which makes it resume transmitting where it left off.

A second type of protocol, DTR Handshake, is available to control data-stream to the printer. When this protocol is in effect, the printer deasserts Data Terminal Ready when the receive buffer is nearly full, causing the S/10 to stop transmitting. When the receive buffer is nearly emptied, the printer reasserts the pin, causing the S/10 to resume transmitting. The S/10's pin 20 (Clear to Send) should be connnected to Data Terminal ready on the printer (normally the printer's pin 20) when the protocol is in use. In most situations this can be achieved by a straight pin-to-pin connection. DTR Handshake protocol can be selected by altering the first field of Status Line Three to read $\pm$dtr or both.

If the printer does not recognize either of the above protocols, it may still be possible to achieve successful printing by setting the transmit baud rate so low that the buffer never overflows. The printer port baud rate is set using the rightmost field of Status Line Two.

The S/10 does not respond to ETX/ACK/NAK signals. However, most printers that use this protocol can be set to use one of the other two protocols. For printers that use only ETX/ACK/NAK protocol, the only recourse is to set the transmit baud rate so low that the buffer never overflows.

PIN ASSIGNMENTS - AUX PORT

Following are the auxiliary pin assignments:

PIN		
1	Protective Ground	Chassis Ground
2	Received Data (External Origin)	Used for receiving data from the printer. XON/XOFF codes received will control the S/10's output stream.
3	Transmitted Data (S/10 Origin)	Used to transmit serially encoded data. When no data is being transmitted this pin is held in the mark state.
4		Not used.
5	Data Terminal Ready (S/10 Origin)	Asserted while the S/10 is powered on, even while in Local Mode or long break (the Function and Tab keys).
6	Request to Send (S/10 Origin)	Asserted while the S/10 is powered on.
7	Signal Ground	Establishes the common reference potential for all voltages on the interface. It is permanently connected to the S/10 chassis.
8-19		Not used.
20	Clear to Send (External Origin)	If not connected, it is ignored; if connected, the S/10 expects it to be asserted and will not transmit unless it is.
21-25		Not used.

TABLE OF ASCII CODES

0	00	nul	32	20	sp	64	40	@	96	60	`
1	01	soh	33	21	!	65	41	A	97	61	a
2	02	stx	34	22	"	66	42	B	98	62	b
3	03	etx	35	23	#	67	43	C	99	63	c
4	04	eot	36	24	$	68	44	D	100	64	d
5	05	enq	37	25	%	69	45	E	101	65	e
6	06	ack	38	26	&	70	46	F	102	66	f
7	07	bel	39	27	'	71	47	G	103	67	g
8	08	bs	40	28	(	72	48	H	104	68	h
9	09	ht	41	29	)	73	49	I	105	69	i
10	0A	lf	42	2A	*	74	4A	J	106	6A	j
11	0B	vt	43	2B	+	75	4B	K	107	6B	k
12	0C	ff	44	2C	,	76	4C	L	108	6C	l
13	0D	cr	45	2D	-	77	4D	M	109	6D	m
14	0E	sp	46	2E	.	78	4E	N	110	6E	n
15	0F	so	47	2F	/	79	4F	O	111	6F	o
16	10	dle	48	30	0	80	50	P	112	70	p
17	11	dc1 (XON)	49	31	1	81	51	Q	113	71	q
18	12	dc2	50	32	2	82	52	R	114	72	r
19	13	dc3 (XOFF)	51	33	3	83	53	S	115	73	s
20	14	dc4	52	34	4	84	54	T	116	74	t
21	15	nak	53	35	5	85	55	U	117	75	u
22	16	syn	54	36	6	86	56	V	118	76	v
23	17	stb	55	37	7	87	57	W	119	77	w
24	18	can	56	38	8	88	58	X	120	78	x
25	19	em	57	39	9	89	59	Y	121	79	y
26	1A	sub	58	3A	:	90	5A	Z	122	7A	z
27	1B	esc	59	3B	;	91	5B		123	7B	{
28	1C	fs	60	3C	<	92	5C	\	124	7C	|
29	1D	gs	61	3D	=	93	5D	]	125	7D	}
30	1E	rs	62	3E	>	94	5E	^	126	7E	~
31	1F	us	63	3F	?	95	5F	_	127	7F	del

GLOSSARY

ABORT - To terminate an operation.

ACCESS - To obtain a document already in the system.

ANSI - The American National Standards Institute, which publishes widely accepted guidelines for the coding and transmission of data.

APPEND - To add as a supplement; to attach.

ARCHIVE - An office file, usually on magnetic tape, used to store infrequently accessed documents.

ASCII - The American Standard Code for Information Interchange. A widely accepted seven or eight bit character code.

AUTOMATIC REPEAT KEY - A key which continues striking as long as it is depressed. Keys except CR, Tab, and those keys on the auxiliary keypad will automatically repeat.

BELL ZONE - In text editing, the point at which a bell rings when the cursor approaches the right margin.

BLOCK - One or more sequential lines of text which you define by start and end points and can move, swap,copy, or delete as a unit.

BOOT - To load the operating system into main memory.

BUFFER - Zone between temporary storage and permanent storage.

CENTER - To place a line or block of text an equal distance from both right- and left-hand margin..

CHARACTER - A letter, number, or any other keyboard symbol you enter, display, or print.

COLUMN - Indicates the cursor's horizontal positon. The ruler is marked off horizontally in increments called columns.

COMMAND - Either your instructions or instructions provided by programs that cause the computer to perform specific functions.

CONTROL KEY - Key in the keyboard which alters information sent to the computer, allowing capability for additional functions.

COPY - To reproduce and move a segment of text from one part of a document to another, leaving the original intact.

CR - Carriage return. To CR, press the key labeled Return. CR controls cursor movement and functions as a key to input or execute commands.

CREATE (A DOCUMENT) - To name, type, and enter a piece of text in the system for the first time.

GLOSSARY (continued)

CURSOR - A blinking rectangle or line indicating your current position on the screen.

DATA PROCESSING _ A programming system designed for manipulating numbers and alphabetic characters, as opposed to manipulating text.

DECIMAL TAB - Automatically aligns columns of numbers by their decimal points.

DEFAULT - To accept a pre-assigned value for specific data.

DELETE - To cancel a character, line, or set of lines.

DISK/DISKETTE - A permanent random access physical storage area for programs and data.

DISPLAY - The information on the screen for viewing; to show the information on the screen.

DOCUMENT - One or more lines of text that can be stored in a document library.

DOCUMENT NAME - A group of up to six characters designated by the document owner to serve as a code for storing and retrieving text.

EDIT - To change the text by deletion, substitution, insertion, or re-arrangement.

ENTER - To introduce data into the system, usually by pressing the Return key.

EMULATION - Process whereby one terminal takes on the personality of another. This allows one system to perform the functions of another system. For example, the S/10 can be made to emulate an ODT to do word processing.

ERROR - Indicates a hardware failure or that something is incorrect in a program or command.

EXECUTE - To perform or carry out required or requested functions (usually by typing in a command and then pressing the Return key).

FIELD - Subdivisoin of a record; for example, the customer's name in a customer record.

FILE - Records which have been grouped togther under one identifying title.

FILECODE/NAME - Alphanumeric name (maximum of three characters) you assign to a group of related records.

FILL - A function key which saves keystrokes by repeating a specified character to the end of the line.

FIRMWARE - Program instructions that are part of the computer hardware and interact with the software.

GLOSSARY (continued)

FOOTER - Text formatted to appear automatically at the bottom of the page.

FORMAT - A set of specifications such as tabulations, which determines the final form of a document.

FORMULA - A mathematical statement or equation which can be created, stored, and called up to execute.

GLOSSARY - In OMS Word Processing, a series of keystrokes which can be defined and stored, and later recalled and executed.

HARDCOPY - System output in permanent form (usually on paper), rather than temporary form (screen display).

HARDWARE - Terminals, printers, CPUs, and other physical equipment that make up a computer system.

HEADER - Text formatted to appear automatically at the top of the page.

HOME POSITION - First character position available on the screen (usually upper, left-hand corner).

ID - The name you enter (usually your given name) to gain access to the processor.

INPUT - To enter information into a system.

INSERT - To place data from a filecode into a body of text, not just a filecode, at a specified location.

JUSTIFY - To cause text to print with even left and/or right margins. (Newspaper columns are both left-and right-jutified.)

KEYED SORT - Arranges data in ascending or descending alphabetical or numerical order.

LIBRARY - A storage area identified by a name up to six characters where you can group or organize documents.

LINE CALL - Ability to move the cursor to any line of text within the document.

LOG OFF - To sign off the processor, ending use.

LOG ON - To sign on the processor, beginning use.

MATCH CODE - Identifier used to access a unique record or a group of records in a file.

MEMORY - Area within the computer where commands and data are stored in the system.

GLOSSARY (continued)

MENU - A displayed list of operation choices.

MERGE - In editing, to append or add segments of text ot each other, filling excess space and adjusting to existing margins.

MODIFY - To print, copy, delete, paginate, change description, or rename. To modify is to change document text.

MOTOR BARS - Four bars on the keyboard which control cursor movement and screen brightness. They are also used to access certain information on the system.

MOVE - To transfoer a segment of text from one part of a document to another.

ODT - Office Display Terminal

OPERATING SYSTEM - Software controlling the operations of the system, e.g., CP/M or BB/M. Includes manipulation of stored data and running programs.

OUTPUT - Information processed by a computer system.

OVERLAY - Allows user to replace existing text or spaces with new text.

OVERPRINT - At printout, allows you to overstrike two lines of text that appear separately on the screen.

OWNER - Author or originator of a document.

PAGE CALL - Allows you to display any page of a document.

PAGE CUT - When executed, all text below the cursor shifts to a new page.

PAGINATION - Allows you to define format of pages, e.g., length, margins.

PASSWORD - The unique set of characters you use to gain access to the system. A password is confidential to insure security.

PITCH - Number of characters per horizontal inch of type. Pica type is 10-pitch; elite, 12-pitch.

PRINT - To produce a hardcopy of data.

PROMPT - A displayed suggestion or request for response.

QUEUE - A list of documents waiting to be processed or printed.

RECORD - Collection of logically related data elements or fields. A collection of records, then, makes up a data file.

RESTORE - To return an altered or destroyed line of text to its previous appearance. You must do this before entering any new information into the system.

GLOSSARY (continued)

RETRIEVE - To find data (usually a document) on a disk and bring it into the main memory of a computer.

RULER - An information line at the top of the screen containing margin and tab settings and header and footer commands.

SCROLL - To adjust the screen image vertically or horizontally to bring data beyond screen boundaries into view.

SCROLLING REGION - The part of the screen which can be scrolled while other parts remain stationary.

SECTOR - Subdivision of a track on a disk. Each sector on a track is marked so that it is readily available.

SECURITY SYSTEM - Prevents information from being accessed by unauthorized persons and compiles system user reports (SAC).